

VER : 1A
PWA:
PWB:

FAN & THERMAL
EMC2112 PG 37

REGULATOR	
+1.5V_SUS/+0.75V_DDR_VTT	PG 46
+1.05V_VTT	PG 47

CPU VR	PG 43
DC/DC +3.3V_ALW/+5V_ALW/ +15V_ALW	PG 44
VGA Core	PG 49




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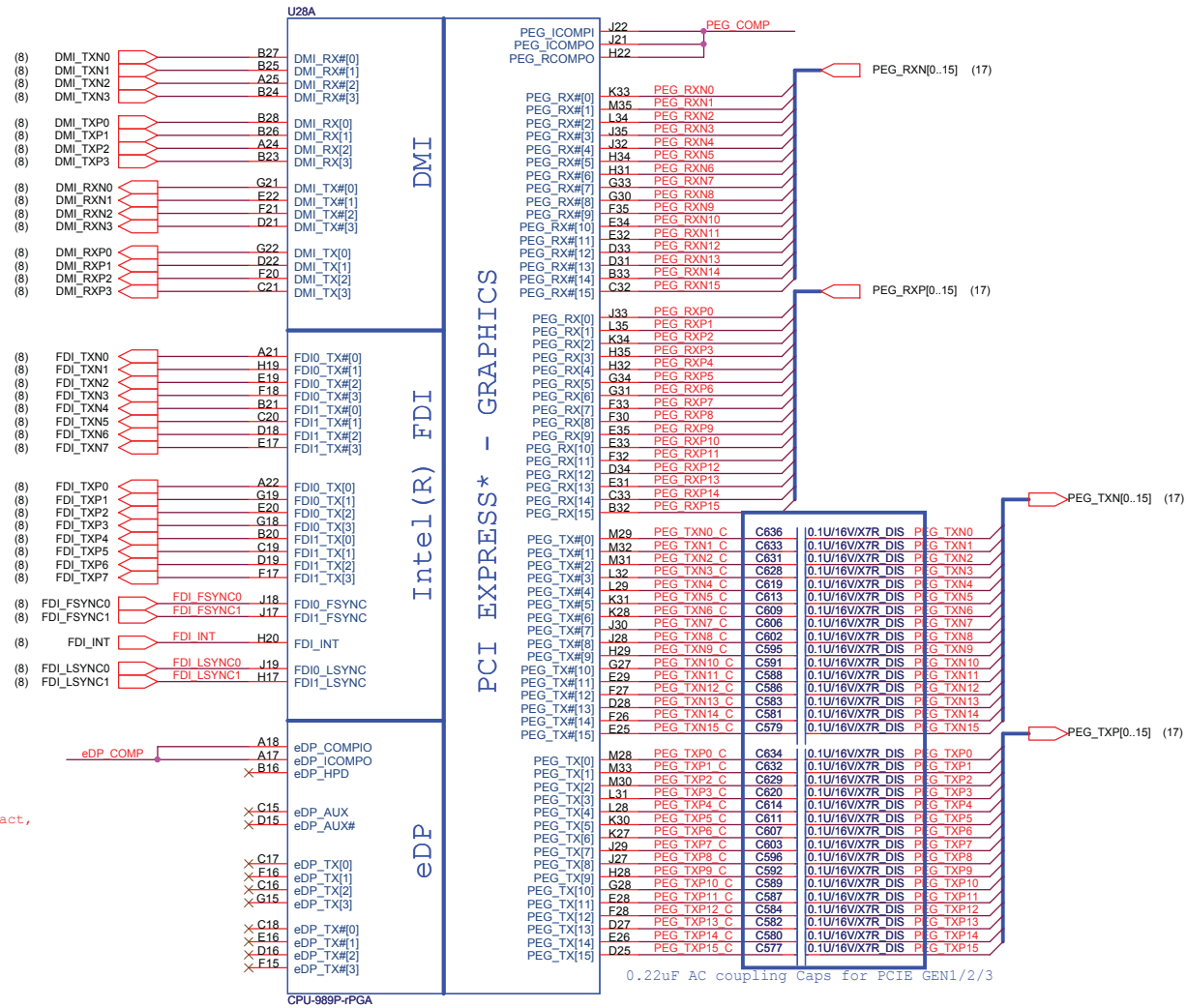
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-7	Sandy Bridge
8-14	PCH
15-16	DDRIII SO-DIMM(204P)
17-21	N12P-GE/N12P-GT
22-23	VRAM
24	LCD CONN
25	HDMI CONN
26	MINI DP CONN
27	Card Reader (JMB389)
28	SIO (ITE8502)
29	MINI-Card (WLAN/WPAN)
30	MINI-Card (WWAN)
31	LAN(RTL8111EL/RJ-45)
32	Right PUSB/ESATA
33	SATA (HDD & ODD)
34	TP / KEYBOARD
35	SWITCH / LED / T-Screen
36	FLASH / RTC/ RESET CIRCUIT
37	FAN / THERMAL
38	AUDIO CODEC
39	AUDIO AMP
40	Left USB/MMB CONN
41	BLANK
42	Charger (ISL88731)
43	CPU CORE(NCP6131S)
44	3V/5V (TPS51427A)
45	1.8V_RUN(RT8015DGQW)
46	1.5_DDR/0.75(RT8207A)
47	1.05V_VTT(VT358)
48	VCCSA(TPS51461)
49	VGA_N12x-dGFX(NCP3218MNR)
50	Run Power Switch
51	DCin & Batt
52	PAD & SCREW
53	SMBUS BLOCK
54	THERMAL MAP
55	Power Block Diagram
56	Power sequence Block
57	power sequence(DIS)
58	power sequence(UMA)
59	power sequence(OPTIMUS)

Power States

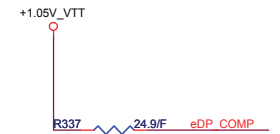
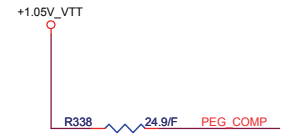
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,52,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+5V	13,33,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,13,14,19,24,28,29,37,41,42,44,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30,31,32,33,35,37,38,39,40,41,42,46,51,52,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.8V_RUN_GFX	+1.8V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	35	MOD Power	MODC_EN	
+5V_HDD	+5V	35	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,60	CPU POWER	RUN_ON	
+1.1V_GFX_PCIE	+1.1V	18,50	VGA POWER	GFX_ON	

GND PLANE	PAGE	DESCRIPTION
 GND	ALL	

Sandy Bridge Processor (DMI, PEG, FDI)



DP & PEG Compensation

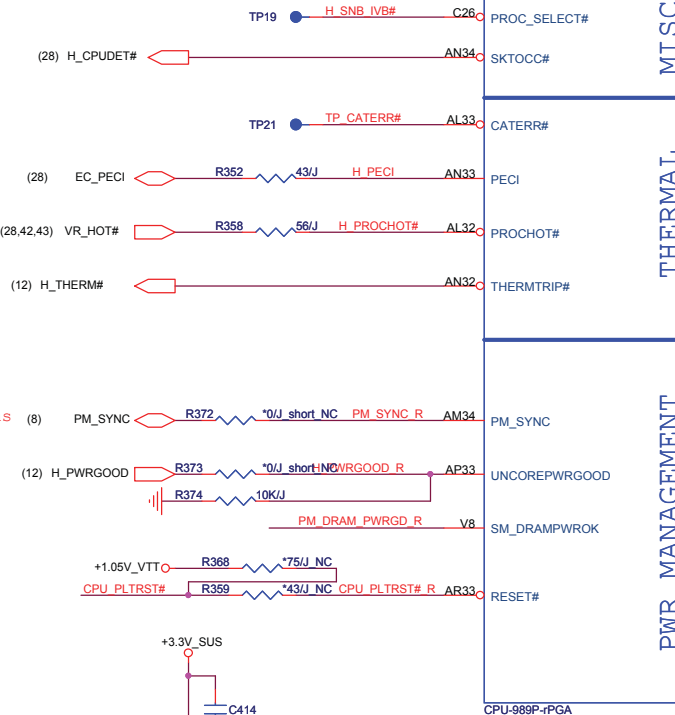


- DG (V0.5) P66:
- FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1] can be tied to GND (through 1K \pm 5% resistors); In addition, can be ganged together with one resistor [1K \pm 5% resistors].
 - If left as no connect, there is no functional impact, but power (~15mW) may be wasted.



Sandy Bridge Processor (CLK,MISC,JTAG)

WW31.MOW Page 5 (SNB_IVB# N.A at SNB EDS #27637 0.7v1)



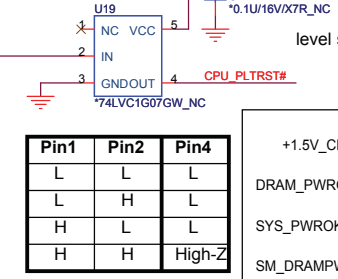
	DIS	SW
Ra	NA	0 ohm
Rb	1K ohm	NA
Rc	1K ohm	NA

shut down when asserted
Over 130 degree C will drive low

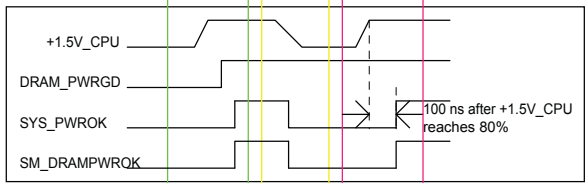
provide power management status (form PCH to CPU)

IN	OUT
L	L
H	High-Z

(11,17,27,28,29,30,31,40) PLTRST#

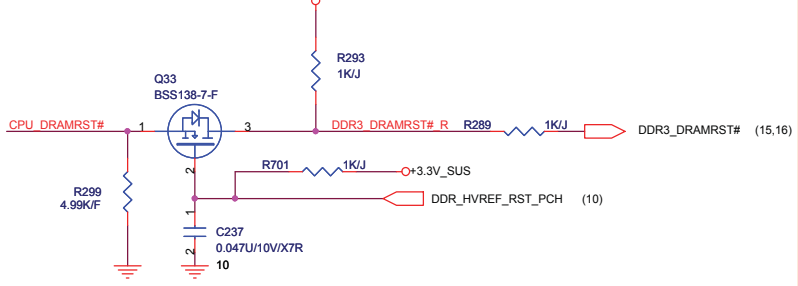


Pin1	Pin2	Pin4
L	L	L
L	H	L
H	L	L
H	H	High-Z

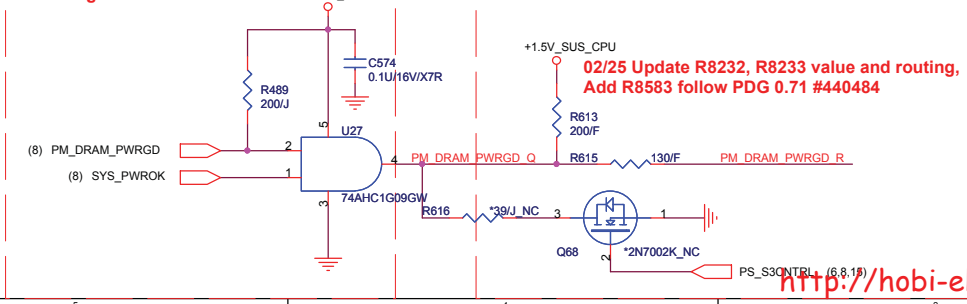


+1.5V_SUS keep DDR3_DRAMRST# high to avoid CPU_DRAMRST# low when into S3 (Because can't reset DRAM when into S3)

S3 Power reduce



3/16 Change topology; Add AND gate based on DG rev0.9



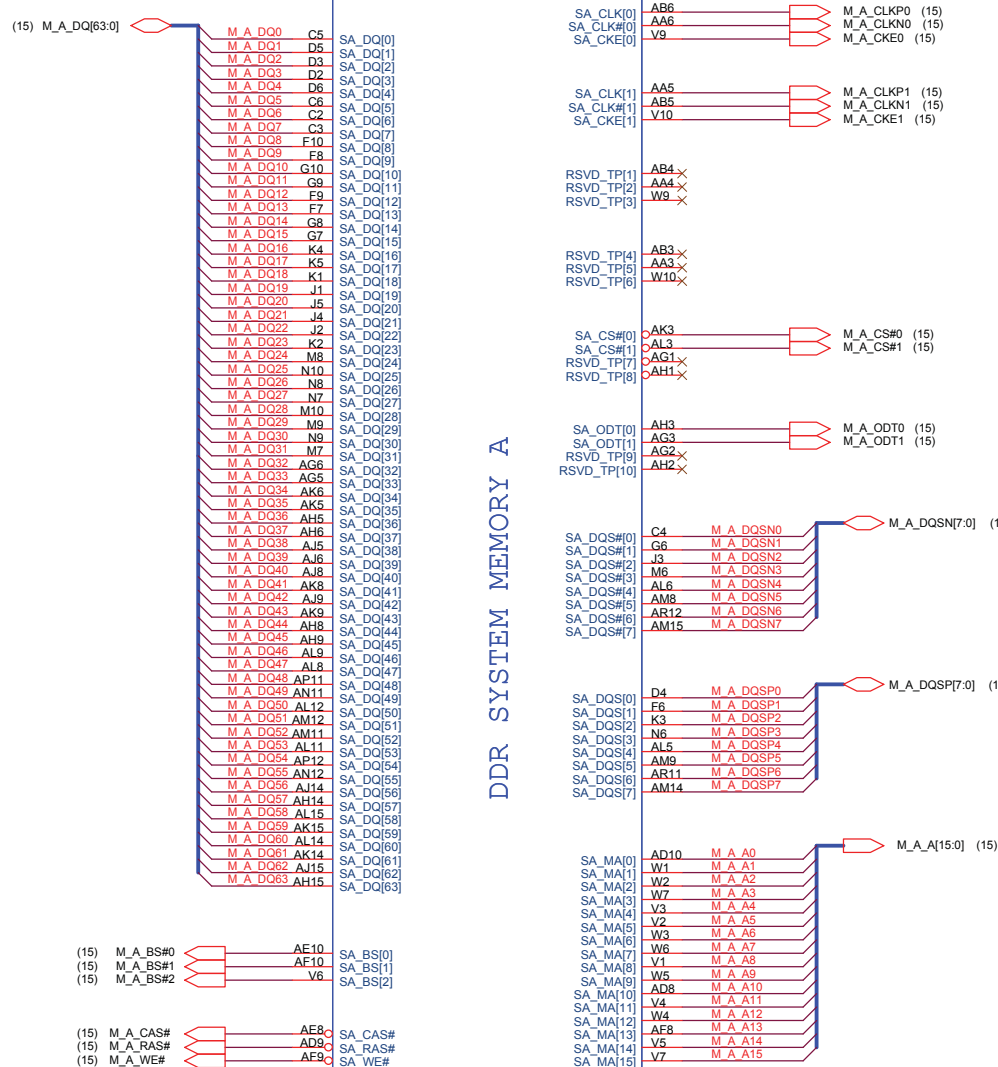
<http://hobi-elektronika.net>

Sandy Bridge Processor (DDR3)

U28C

CPU-989P-IPGA

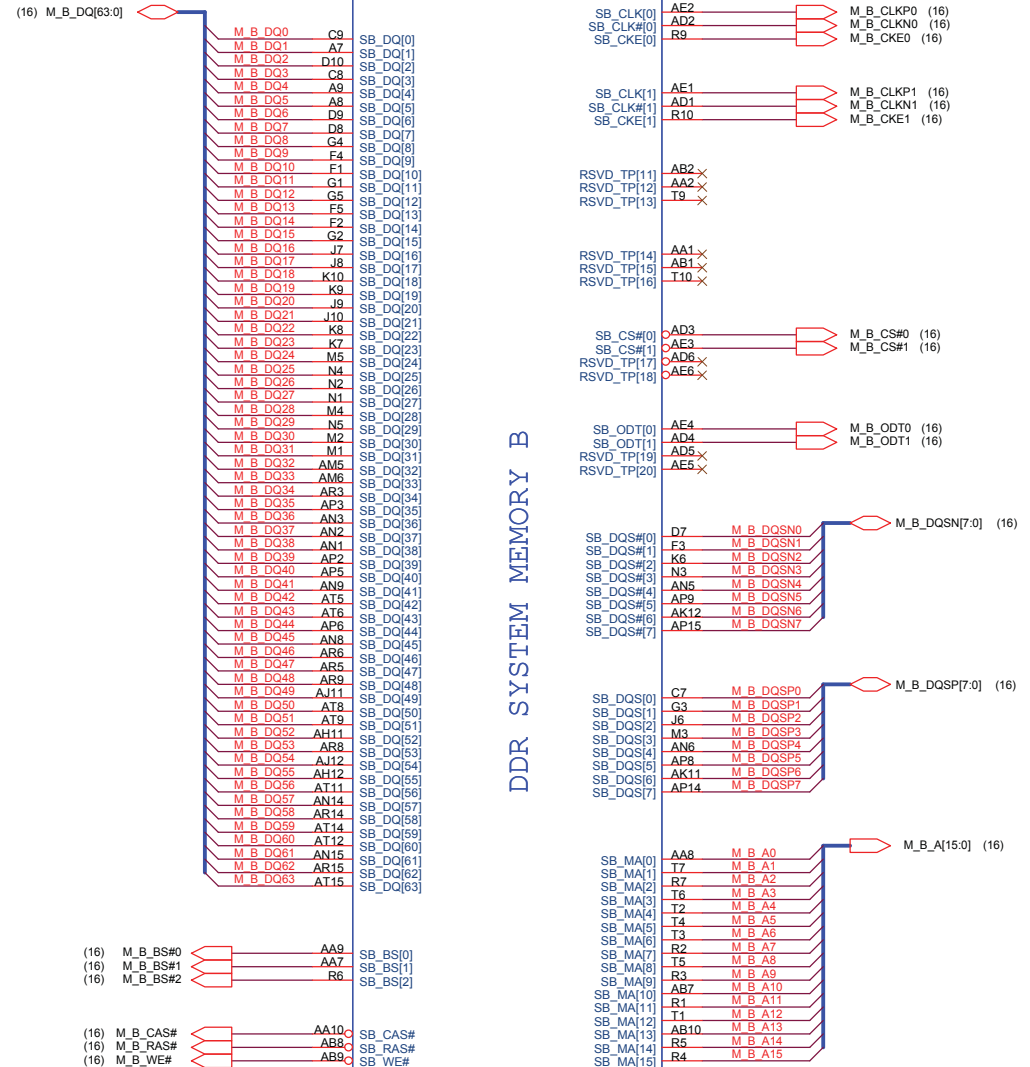
DDR SYSTEM MEMORY A



U28D

CPU-989P-IPGA

DDR SYSTEM MEMORY B



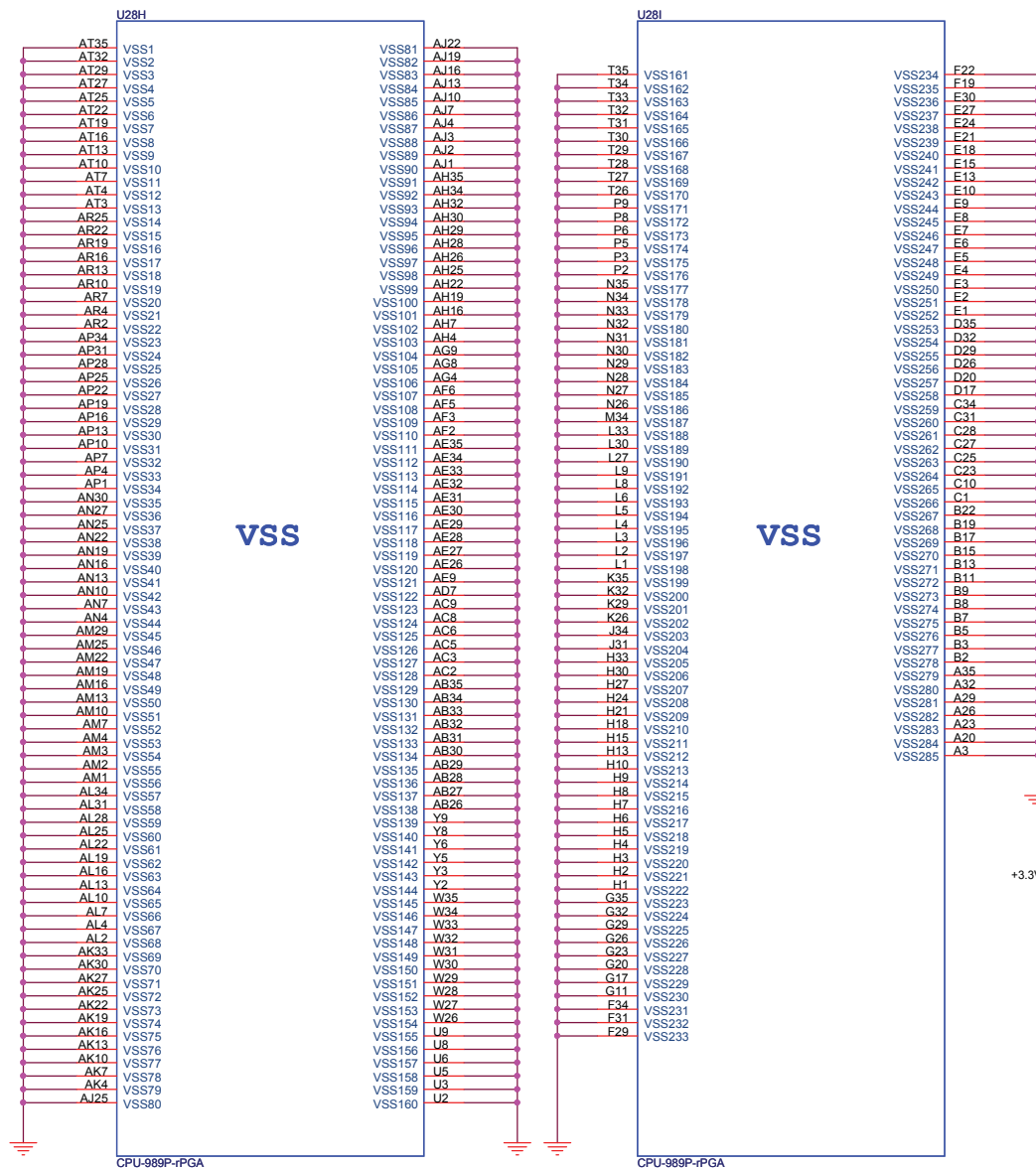
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PROJECT : GM6C MLK DIS

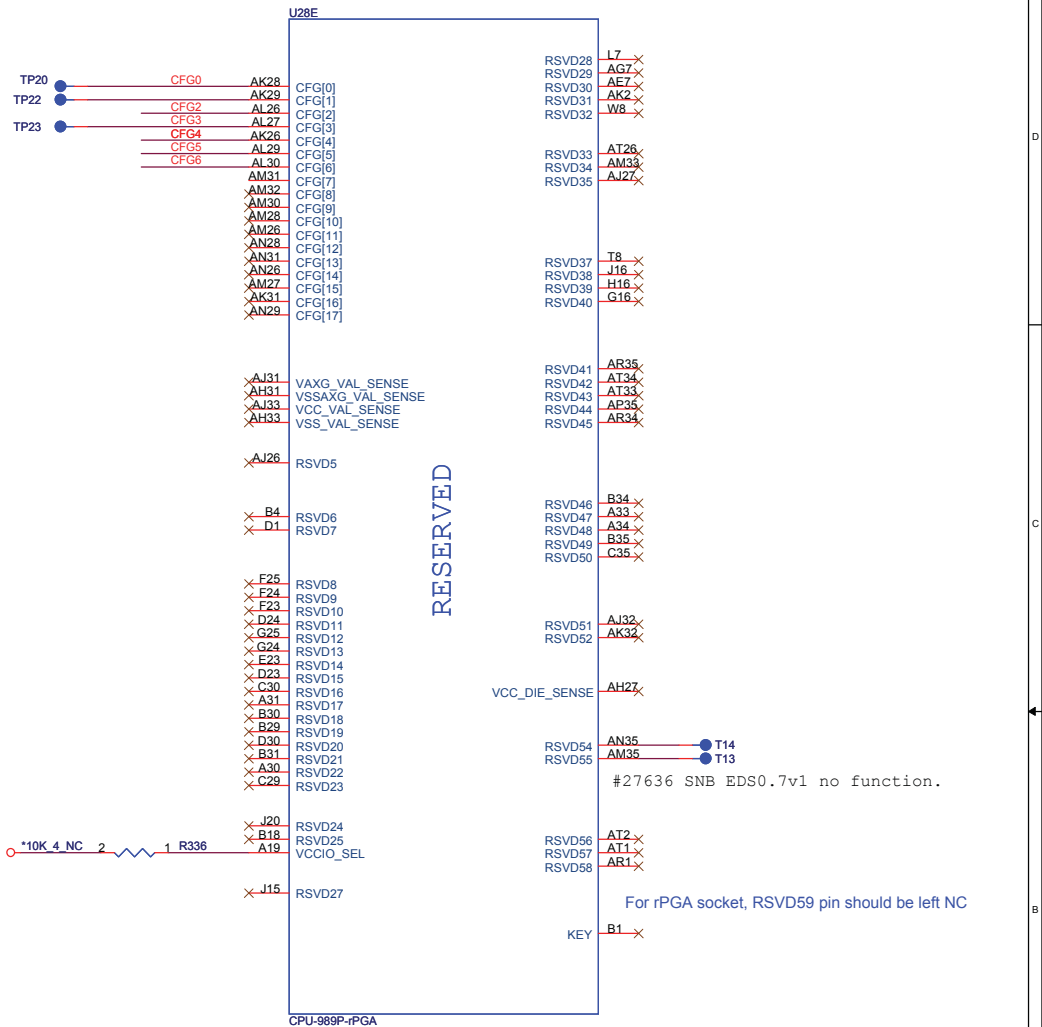
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Date: Friday, January 07, 2011 Sheet 6 of 59

Sandy Bridge Processor (GND)



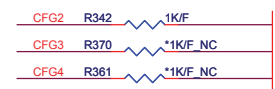
Sandy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Number Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	PCI-E Static x4 Lane Reversal	PEG wait for BIOS training
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP



CFG[6:5] (PCI-E Port Bifurcation Straps)

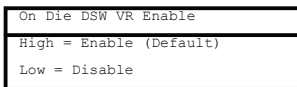
11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



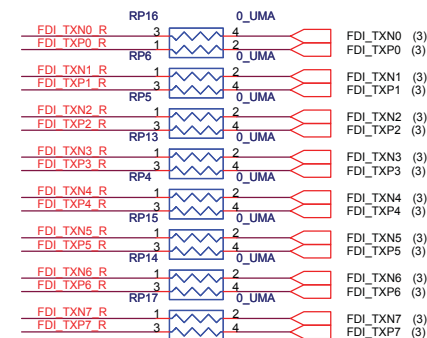
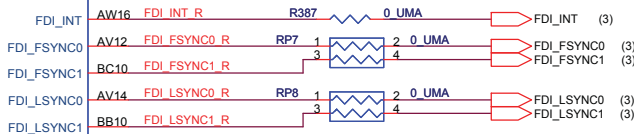
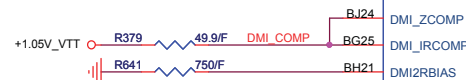
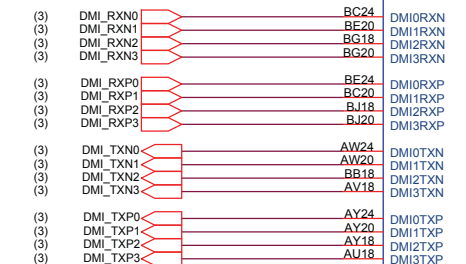
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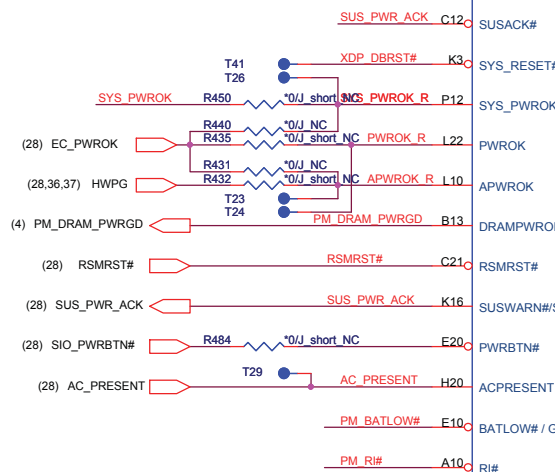
U29C



The schematic diagram illustrates the I/O pin connections for the STM32F405VGT6 microcontroller. The connections are as follows:

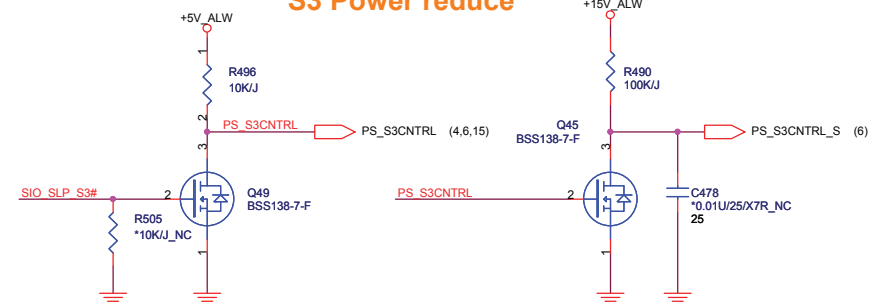
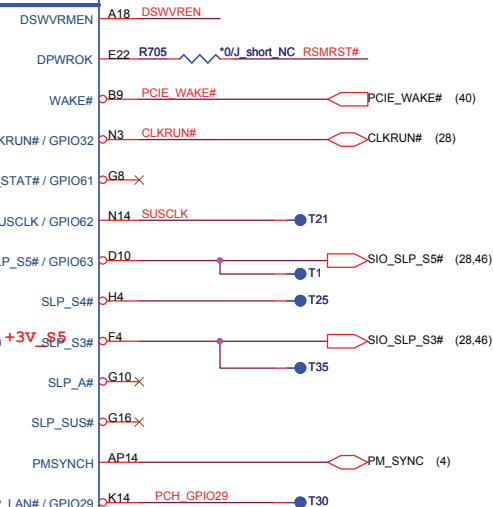
- CLKRUN#**: Connected to **R666** (10K/J), which is connected to **+3.3V_RUN**.
- XDP_DBRST#**: Connected to **R673** (10K/J), which is connected to **+3.3V_RUN**. Additionally, **R674** (*1K/J, NC) is connected to **+3.3V_RUN**.
- RSMRST#**: Connected to **R706** (10K/J), which is connected to **+3.3V_RUN**.
- SYS_PWROK_R**: Connected to **R441** (10K/J), which is connected to **+3.3V_RUN**.
- M_R#**: Connected to **R698** (10K/J), which is connected to **+3.3V_SUS**.
- BATLOW#**: Connected to **R483** (10K/J), which is connected to **+3.3V_SUS**.
- WAKE#**: Connected to **R696** (10K/J), which is connected to **+3.3V_SUS**.
- PWR_ACK**: Connected to **R700** (10K/J), which is connected to **+3.3V_SUS**.
- PRESENT**: Connected to **R479** (*10K/J, NC), which is connected to **+3.3V_SUS**.
- CH_GPIO29**: Connected to **R492** (10K/J), which is connected to **+3.3V_SUS**.

A ground symbol is also shown, connected to the **+3.3V_RUN** and **+3.3V_SUS** lines.



+3V
+3V
+3V
WRDNAC
DS
+3V_
+3V

System Power Management



System PWR_OK(CLG)

(4) SYS_PWROK

U20

TC7SH08FJ

+3.3V_SUS

C469
*0.1U/16V/X7R_NC

EC_PWROK

R447
100K/J

IMVP_PWROK (28.37.43)

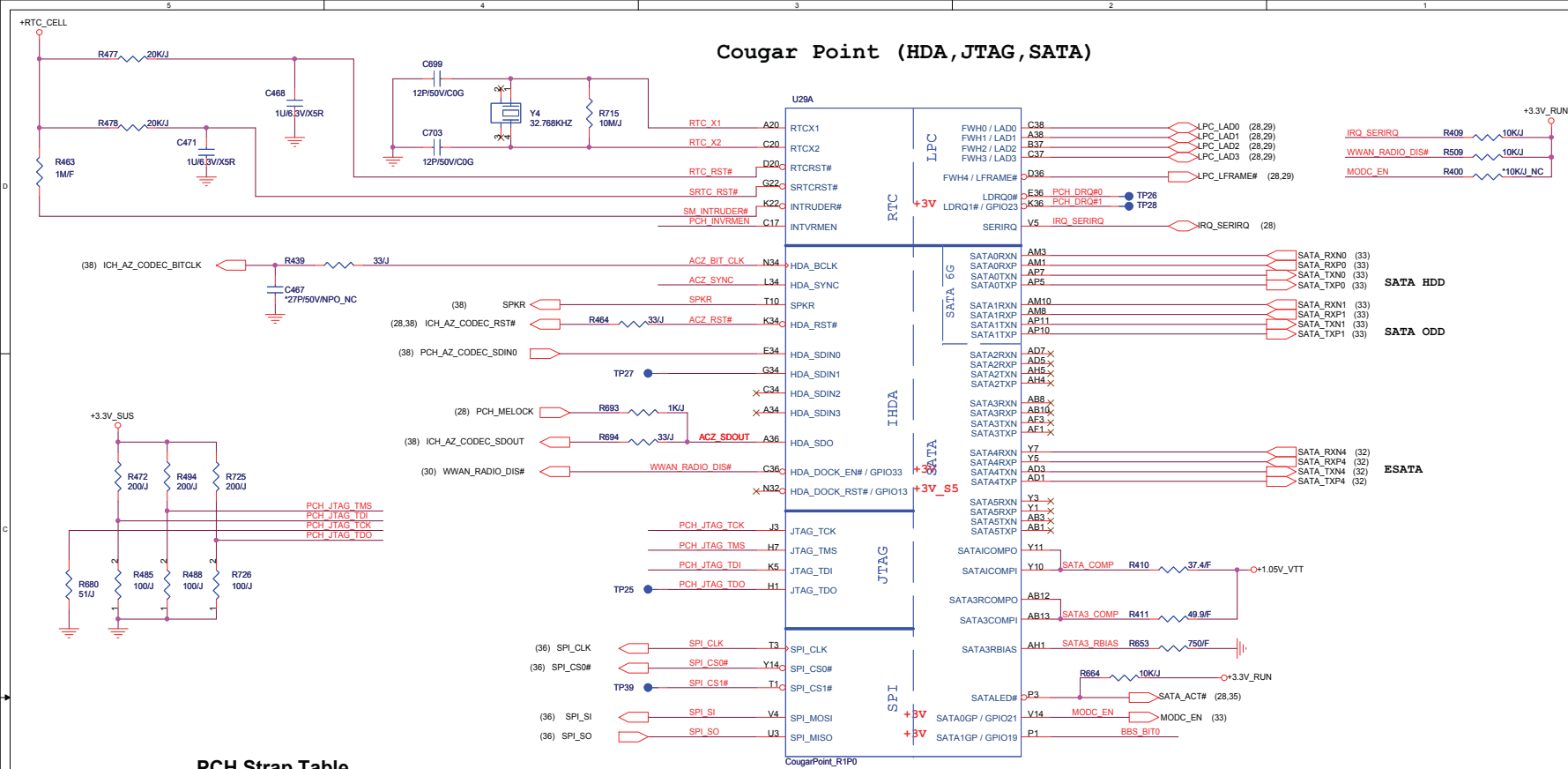


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Cougar Point 1/7

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Cougar Point (HDA,JTAG,SATA)



PCH Strap Table

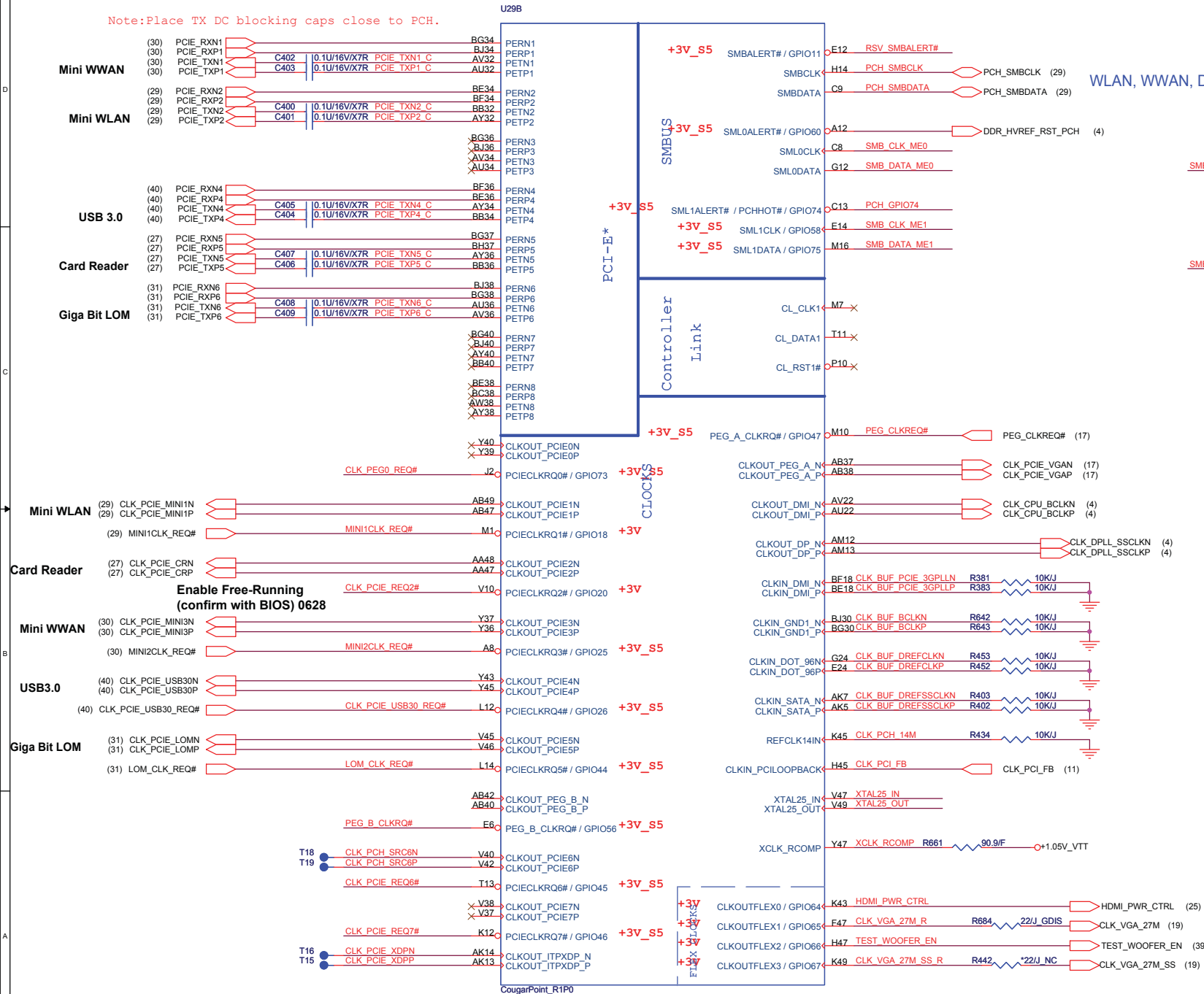
Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_RUN R408 *1KJ_NC SPKR									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R454 *1KJ_NC PCI_GNT3# (11)									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS] R688 *1KJ_NC BBS_BIT1 (11) R665 *1KJ_NC BBS_BIT0
GNT1#	GNT0#	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V										
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3.3V_SUS R892 *1KJ_NC ACZ_SDOUT									
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	+3.3V_SUS R418 *1KJ_NC R424 *10KJ_NC PLL_ODVR_EN (12)									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL R704 *330KJ_NC PCH_INVRMEN									
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm 0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	+1.8V_RUN R392 *2.2KJ_NC DE_T12 (12)									

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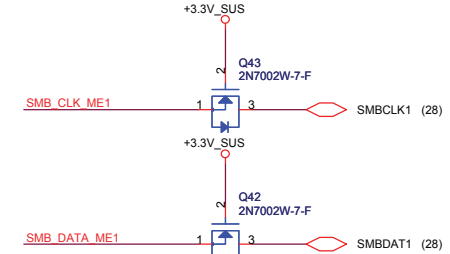
<http://7mobi-elektronika.net>

Cougar Point-M (PCI-E, SMBUS, CLK)

Note: Place TX DC blocking caps close to PCH.

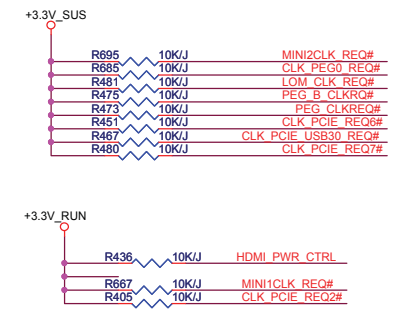


WLAN, WWAN, DIMM0, DIMM1, 3-axis fall sensor



EC

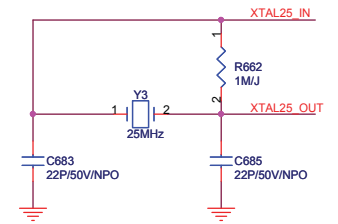
PCIe Clock Request



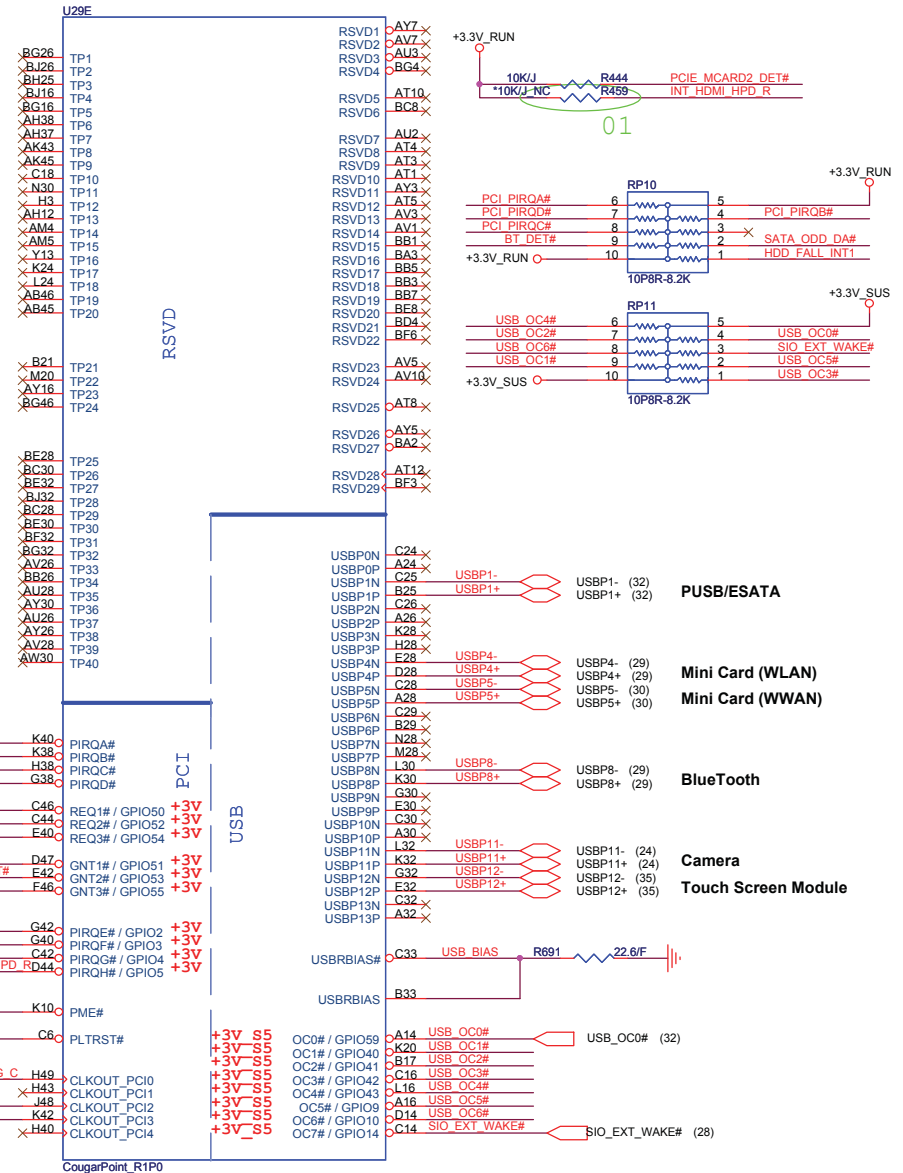
PCI_ECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +V3.3A. PCI_ECLKRQ{1,2} should have a 10K pull-up to +3.3S.

Change as big package (UM9)

25MHz Clock for DCI Function



Cougar Point-M (PCI,USB,NVRAM)

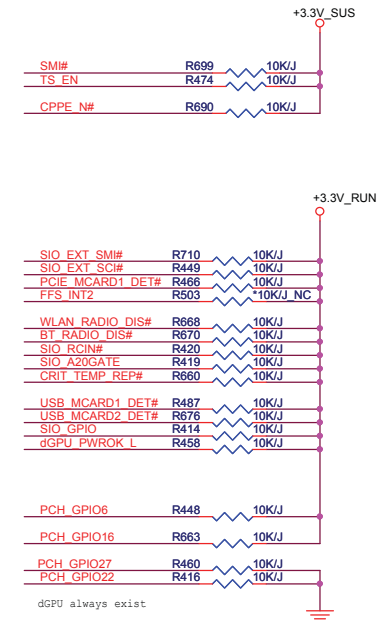
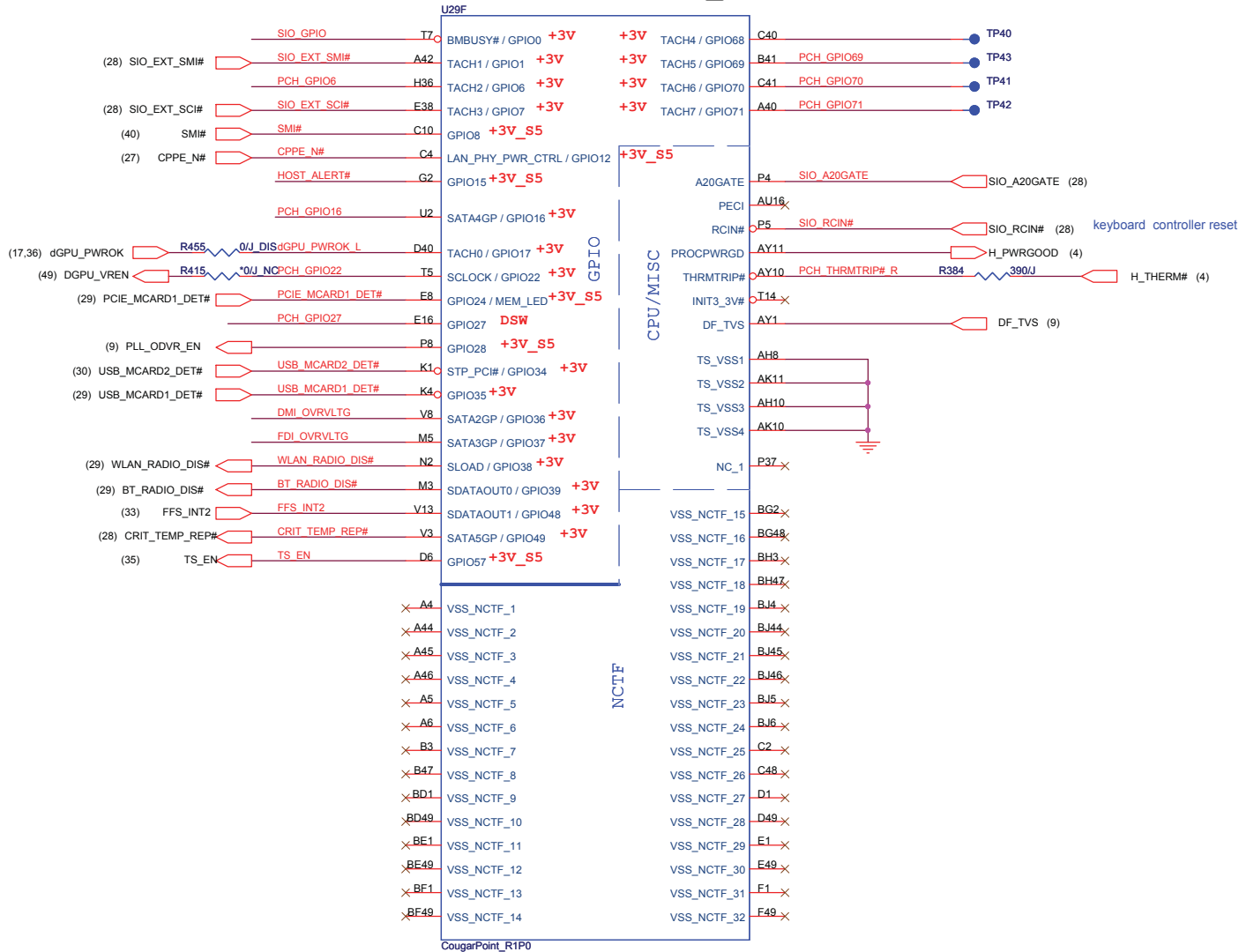


Add Buffers as needed for Loading and fanout concerns.



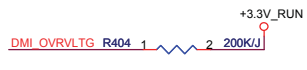
<http://hobi-elektronika.net>

Cougar Point (GPIO,VSS_NCTF,RSVD)



FDI TERMINATION VOLTAGE OVERRIDE

LOW - Tx, Rx terminated to same voltage

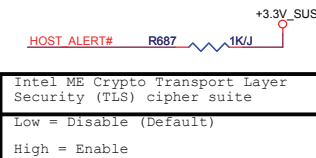


DMI TERMINATION VOLTAGE OVERRIDE

LOW = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

internal PD resistor 20K-ohm
To avoid voltage be divided,
please change GPIO36 PU resistor from
10K-ohm to 200K-ohm. (07/12)

<http://hobi-elektronika.net>



Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)

High = Enable



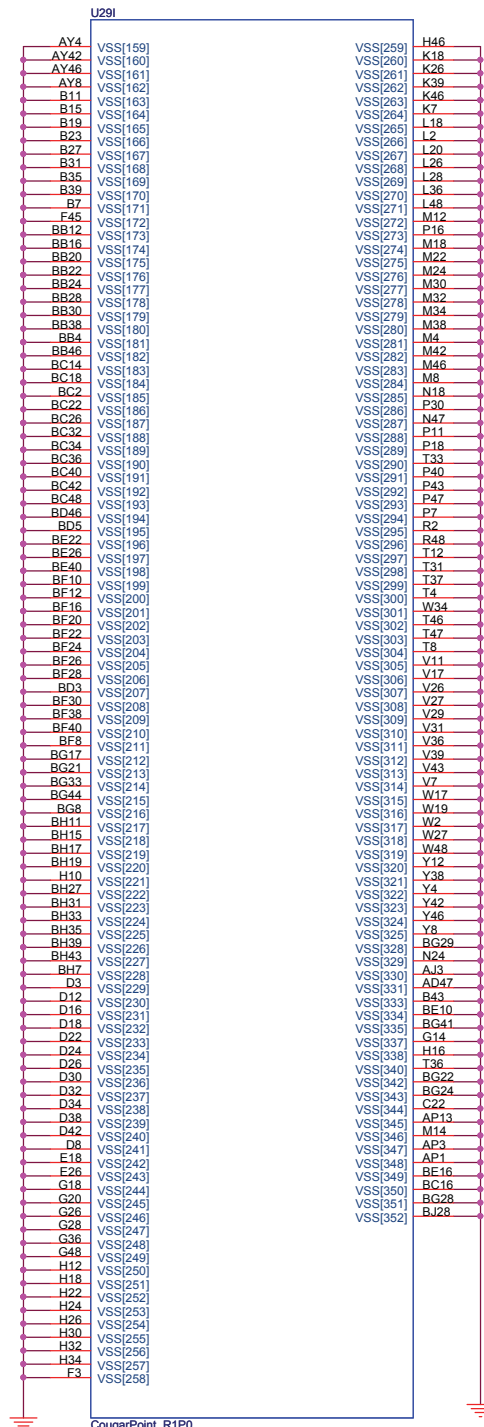
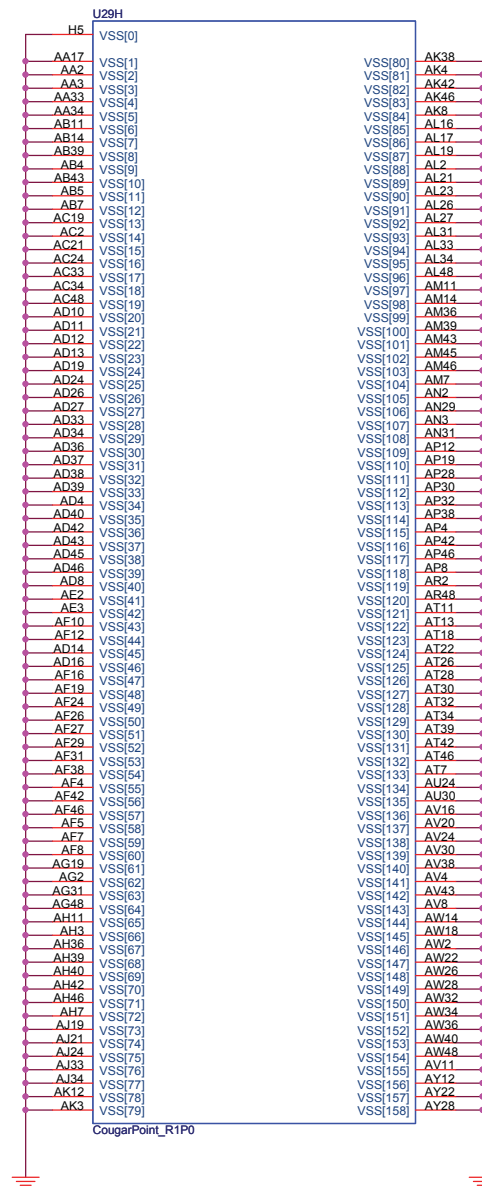
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Cougar Point-M (POWER)



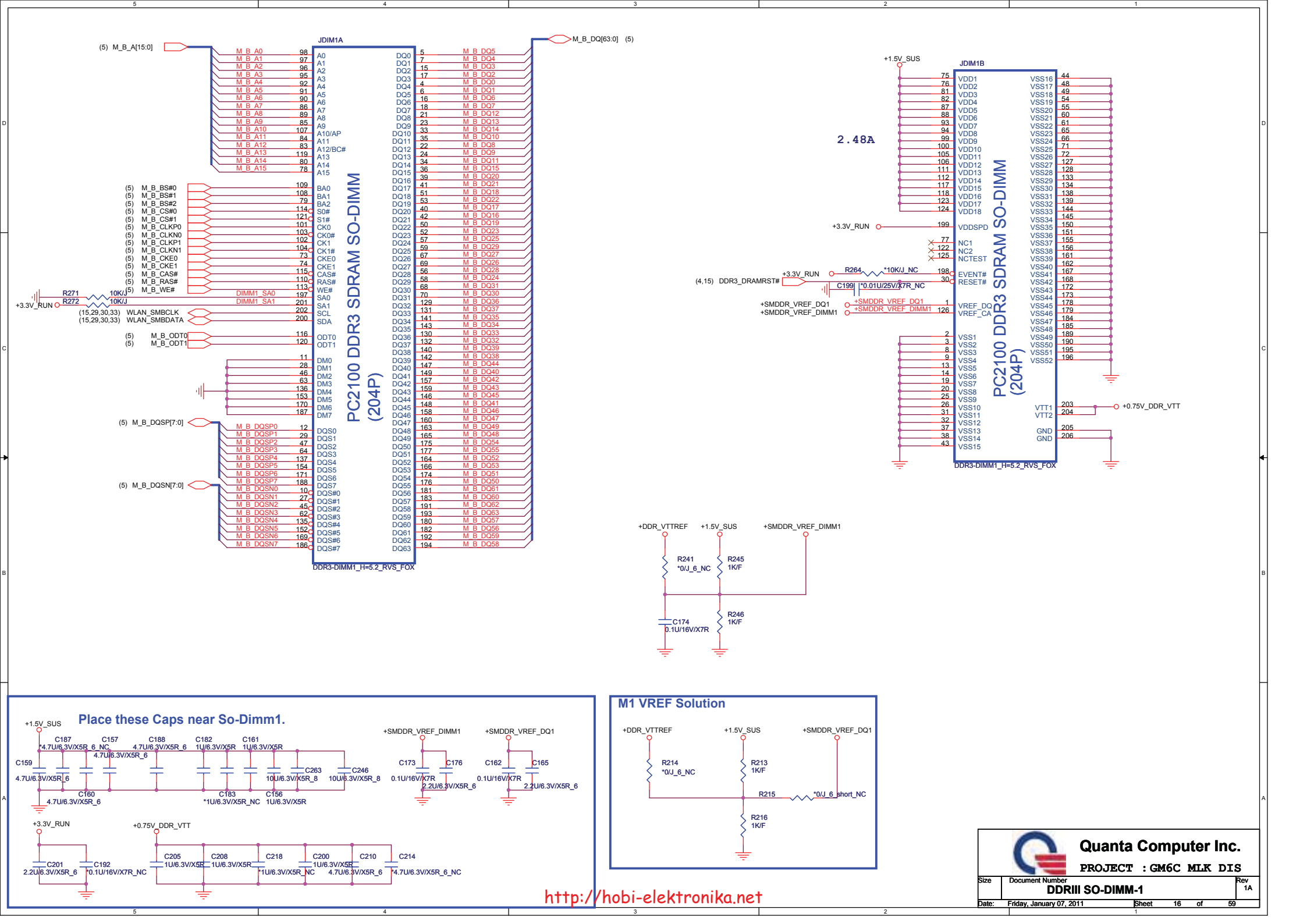
IBEX PEAK-M (GND)



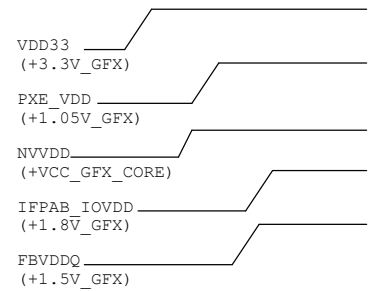
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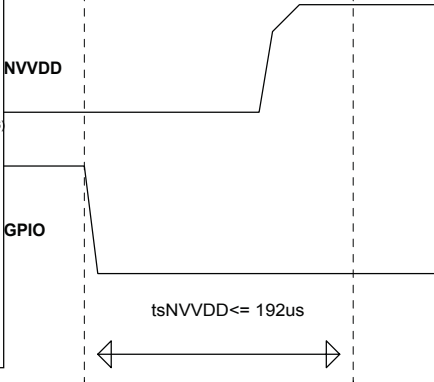
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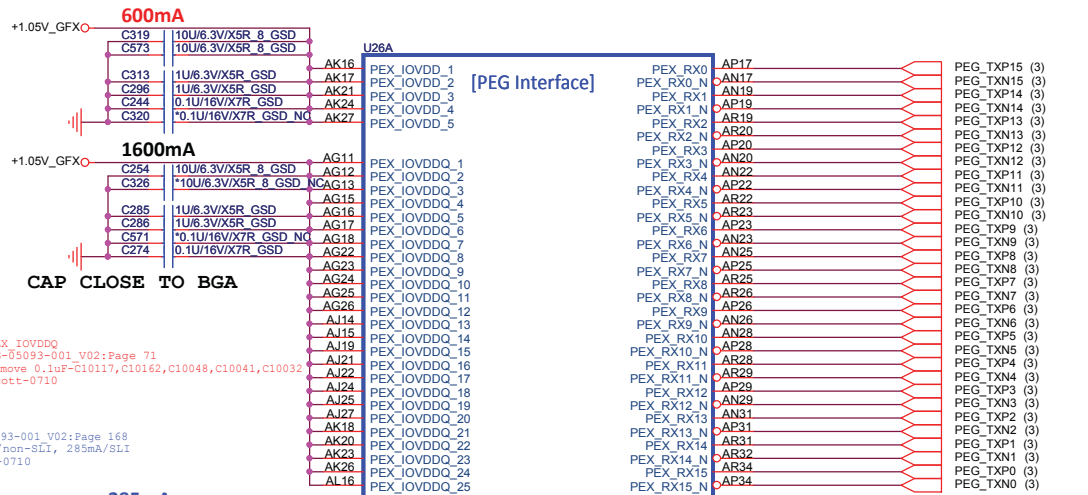
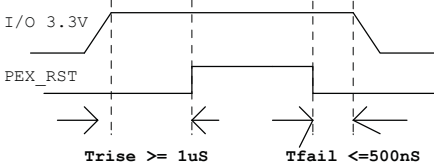
power up sequence



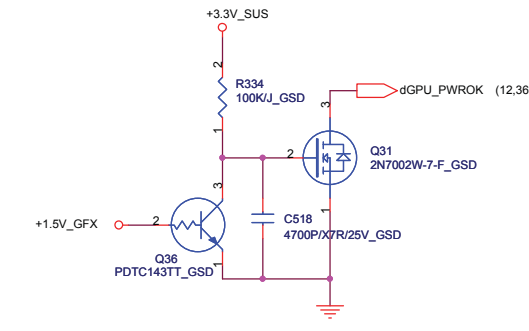
NVVDD Maximum Settling Time



PEX_RST timing



GPU all PWROK



PEX_RST#
DG-05093-001_V02:Page 70
default can be unstuffed
Scott-0711

PEX_CLKREQ_N
DG-05093-001_V02:Page 70
Pull down 2.49K/F
Scott-0711

PEX_TERM
DG-05093-001_V02:Page 70
Pull down 2.49K/F
Scott-0711

TESTMODE
DG-05093-001_V02:Page 207
Pull down 10K
Scott-0711

PEX_CLKREQ# circute is different with GM6.
Confirm with GM6

240mA

24~32 mils width

PEX_PLIVDD
DG-05093-001_V02:Page 71,72
120mA each
Scott-0710



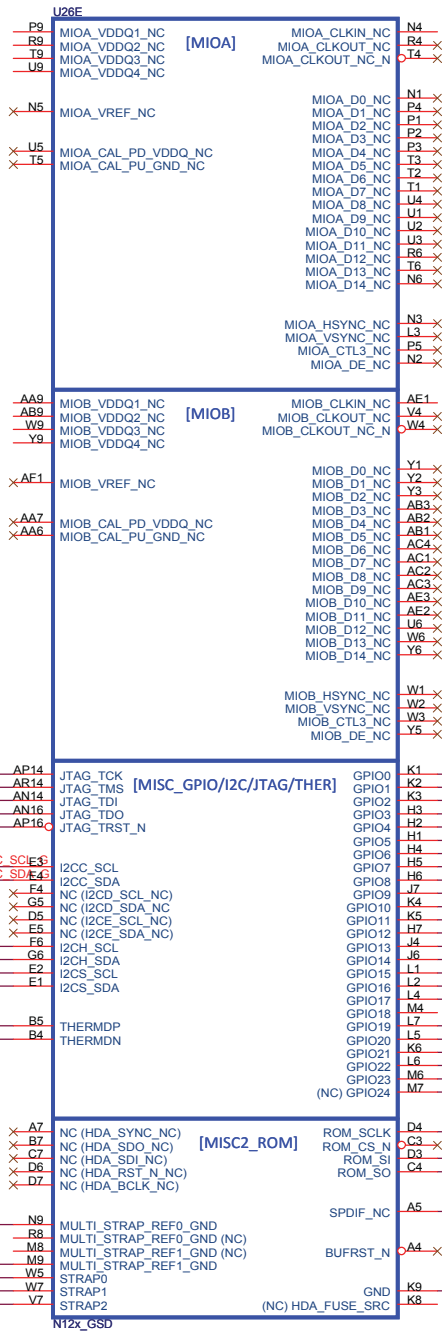
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	DGPU 1/5 (PEG)	1A
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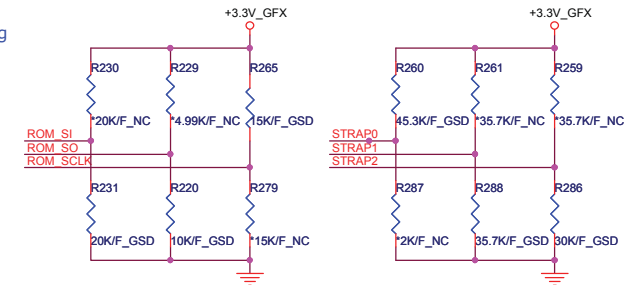
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	X010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	1110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN
0x3(0011)	900MHz 512MB(64M*16) Samsung	AKD5LGHY500		K4W1G1646E-HC11
0x2(0010)	900MHz 512MB(64M*16) Hynix	AKD5LZWTW02		H5TQ1G63DFR-11C
0x6(0110)	900MHz 1GB(128M*16) Hynix	AKD5MGWTW00		H5TQ2G63BFR-11C
0x7(0111)	900MHz 1GB(128M*16) Samsung	AKD5MGWT500		K4W2G1646C-HC11

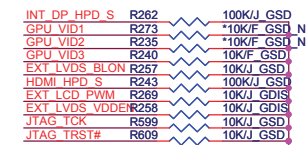
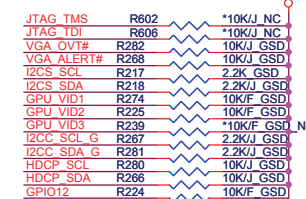
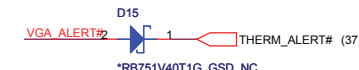
ROM_SI Strap Bit for RAM Mapping

	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111




STRAP2 ROM_SCLK

	PD	30K	PU	15K	0xDF5
N12P-GE (AJON12P0T02)					
N12P-GT (AJON12P0T03)					
N12P-GS (AJON12P0T04)					



GPIO ASSIGNMENTS

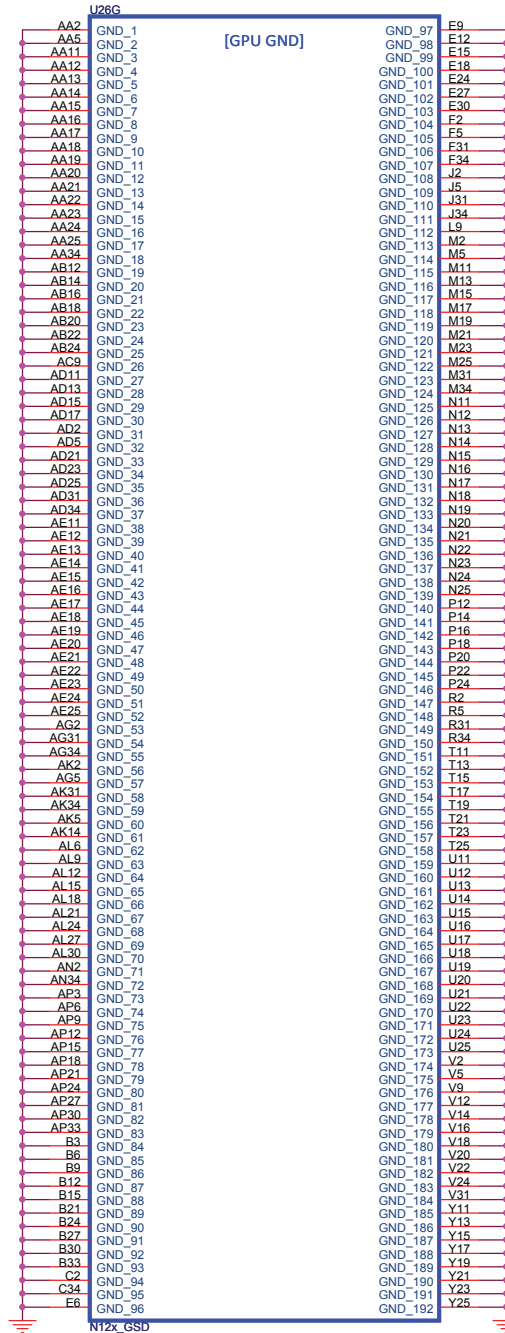
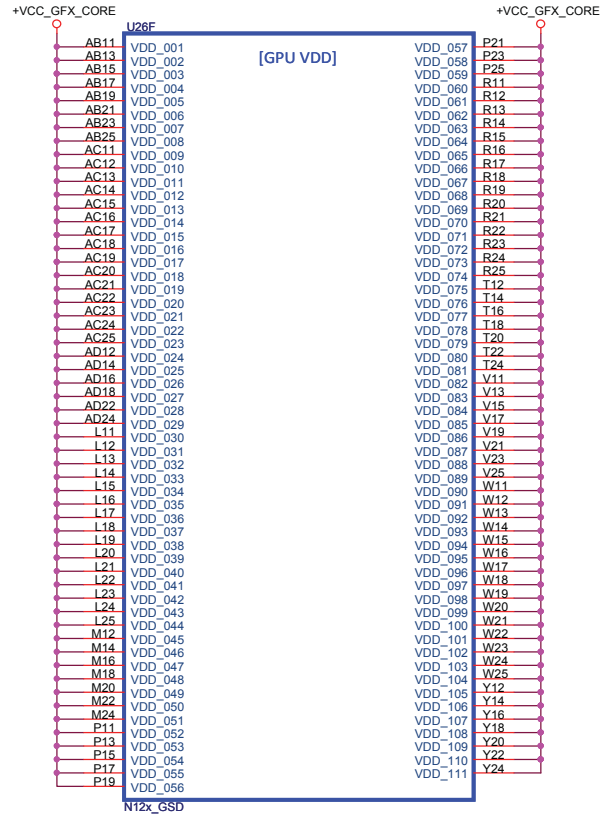
GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	NVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI Raster Sync
12	IN	N/A	AC PWR Detect Input
13	OUT	N/A	Power Supply Control
14	OUT	N/A	Power Supply Control
15	OUT	N/A	Hot plug detect for IFP link E
16	OUT	N/A	Programmable Fan Control
17	OUT	N/A	Reserved
19	OUT	N/A	Reserved
20	OUT	N/A	Hot plug detect for IFP link D
21	OUT	N/A	Reserved
22	OUT	N/A	Hot plug detect for IFP link F
23	OUT	N/A	SLI Swap Ready single
23	OUT	N/A	

 **Quanta Computer Inc.**

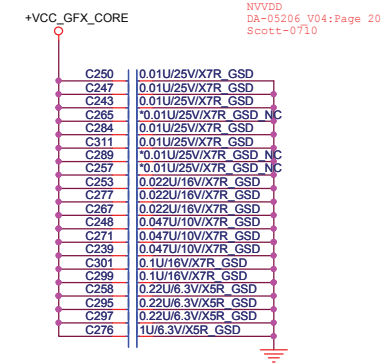
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	DGPU 4/5 (MIO/GPIO)	1A
Date:	Friday, January 07, 2011	Sheet 20 of 59

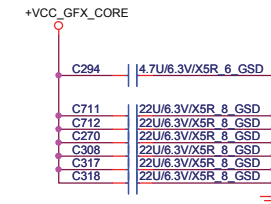
31.56A



PLACE UNDER BALLS

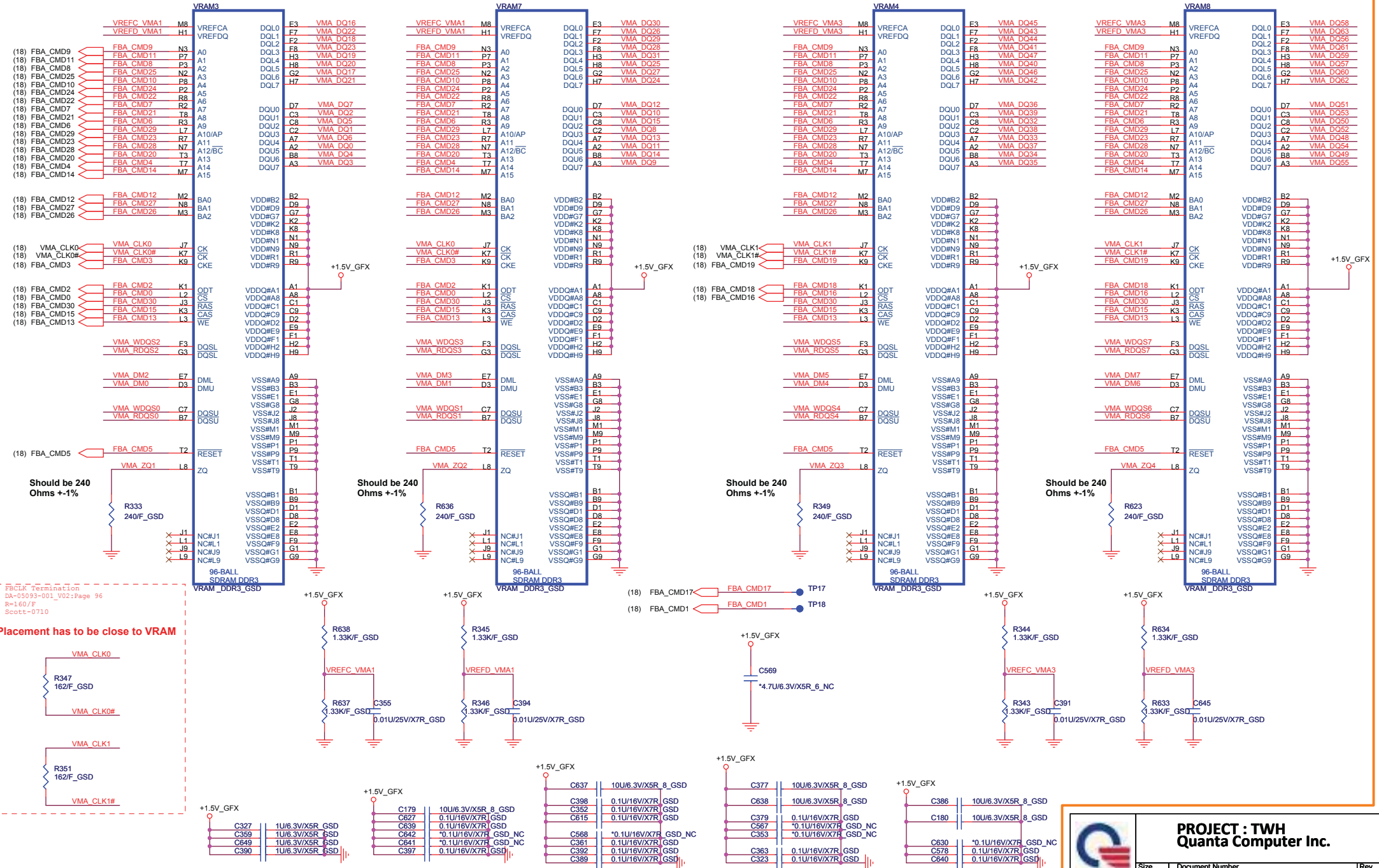


PLACE NEAR BALLS



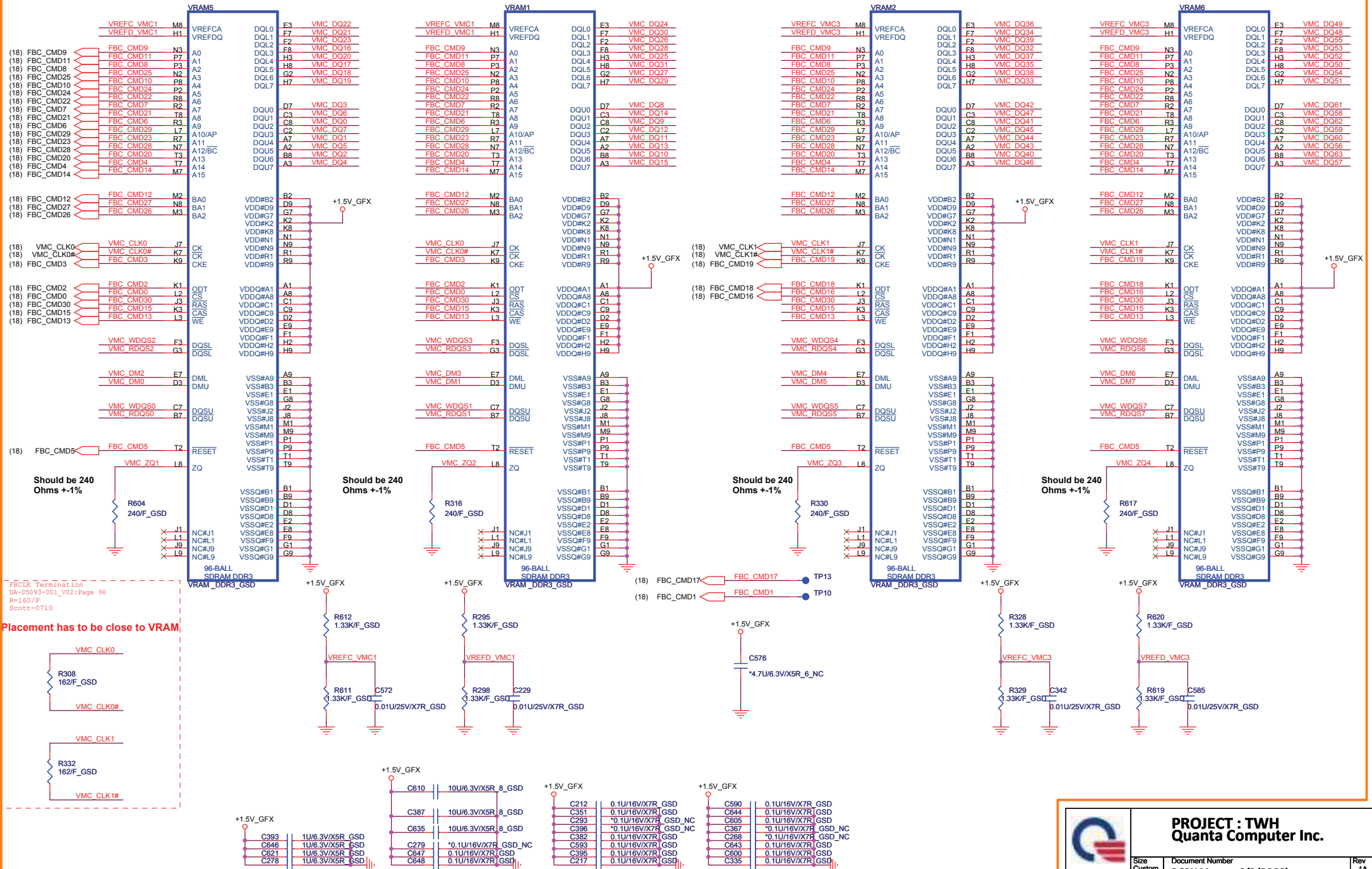
(18) VMA_DQ[63..0]
(18) VMA_DM[7..0]
(18) VMA_WDQS[7..0]
(18) VMA_RDQS[7..0]

CHANNEL A: 256MB/512MB DDR3



(18) VMC_DQ[63..0]
(18) VMC_DM[7..0]
(18) VMC_WDQS[7..0]
(18) VMC_RDQS[7..0]

CHANNEL B: 256MB/512MB DDR3

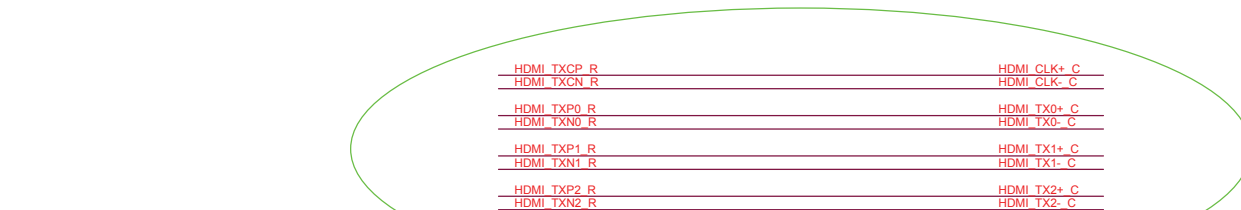
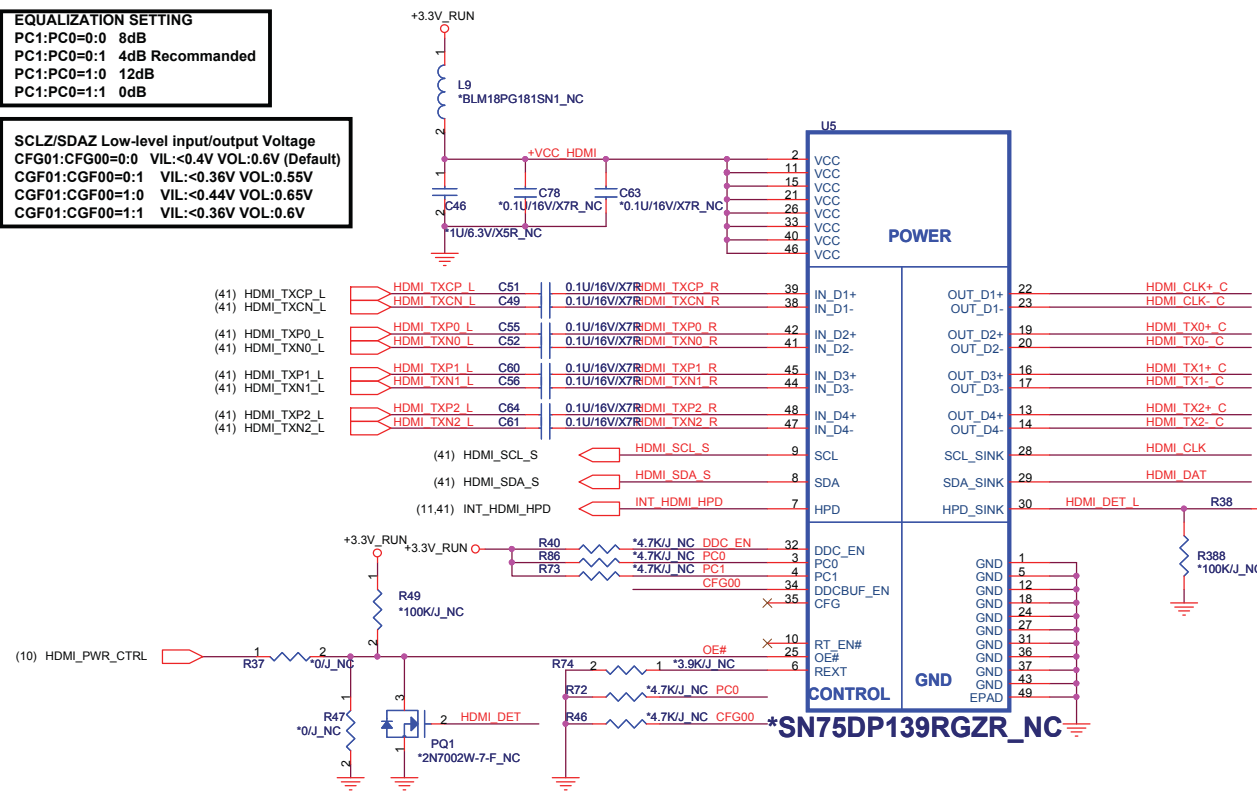


PROJECT : TWH
Quanta Computer Inc.

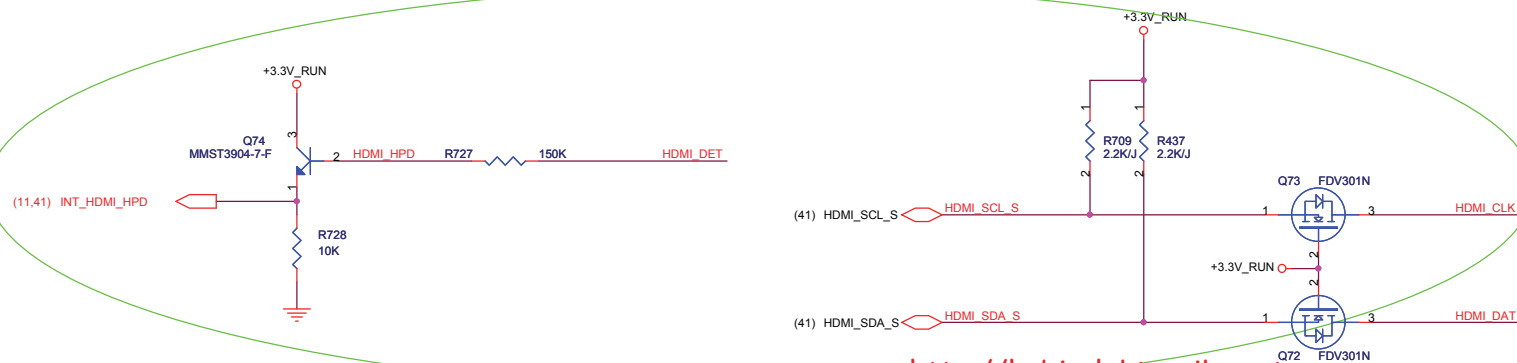
Size	Document Number	Rev
Custom	DGPU Memory 2/2 (DDR3)	1A
Date: Friday, January 07, 2011	Sheet 23 of 59	

EQUALIZATION SETTING
 PC1:PC0=0:0 8dB
 PC1:PC0=0:1 4dB Recommended
 PC1:PC0=1:0 12dB
 PC1:PC0=1:1 0dB

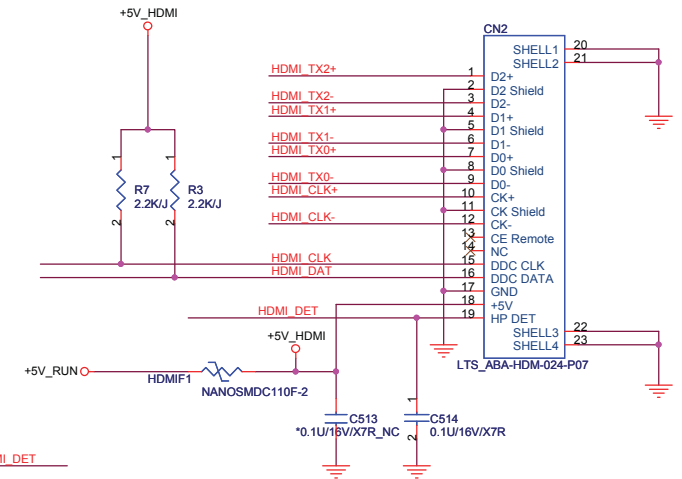
SCLZ/SDAZ Low-level input/output Voltage
 CFG01:CFG00=0:0 VIL:<0.4V VOL:0.6V (Default)
 CGF01:CGF00=0:1 VIL:<0.36V VOL:0.55V
 CGF01:CGF00=1:0 VIL:<0.44V VOL:0.65V
 CGF01:CGF00=1:1 VIL:<0.36V VOL:0.6V



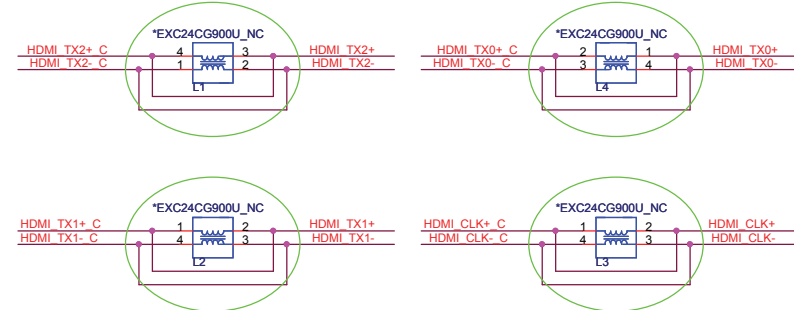
change



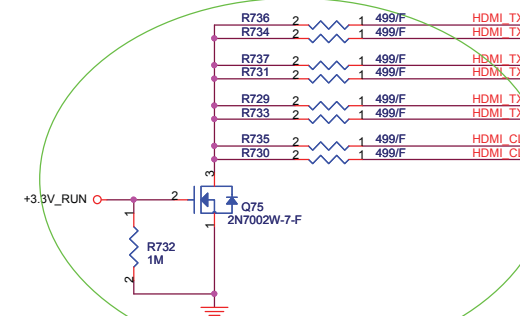
HDMI



Reserve for EMI and close to HDMI CONN



UMA change to 680ohm



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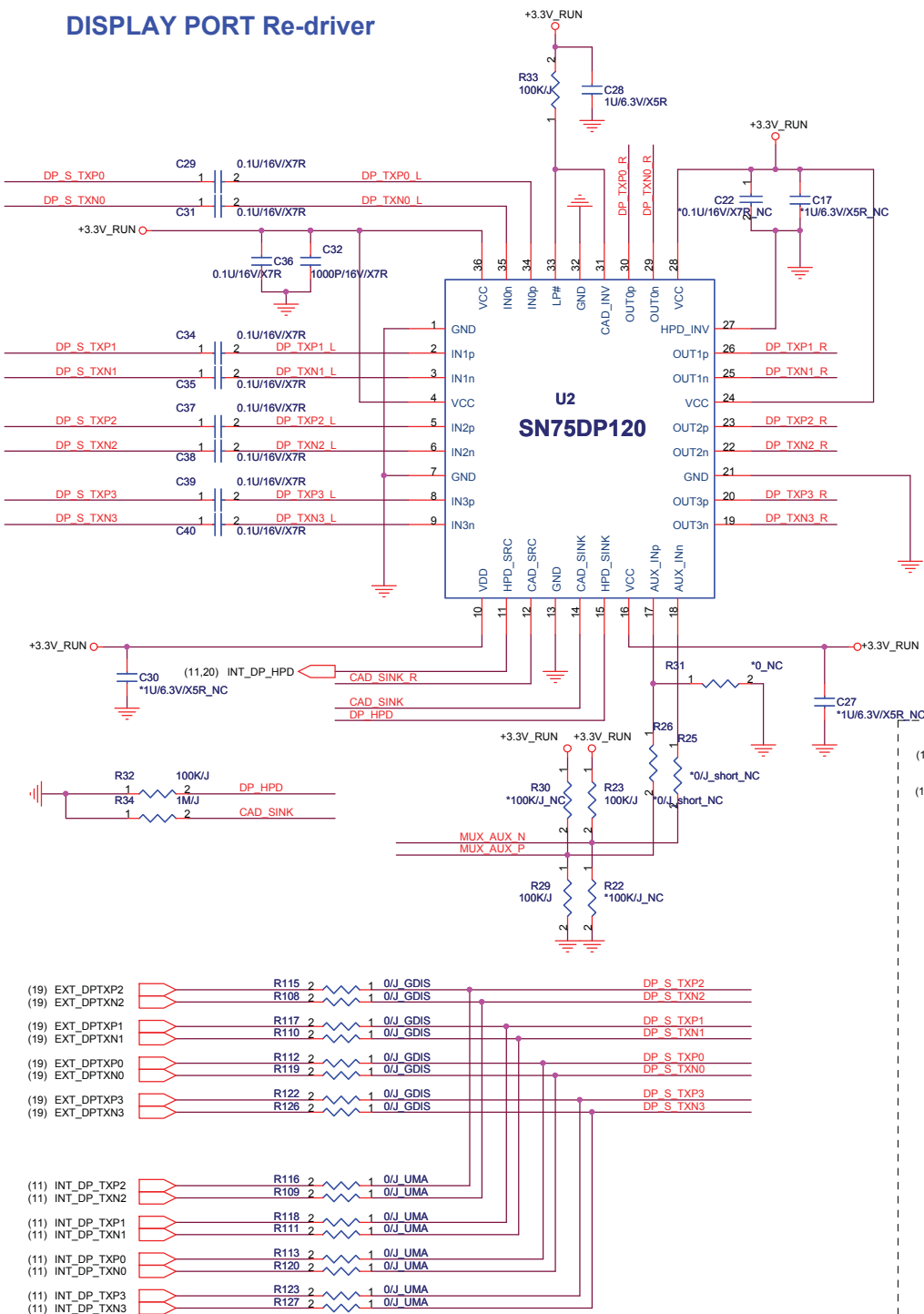
PROJECT : GM6C MLK DIS

Size Document Number
 Date: Friday, January 07, 2011 Sheet 25 of 59

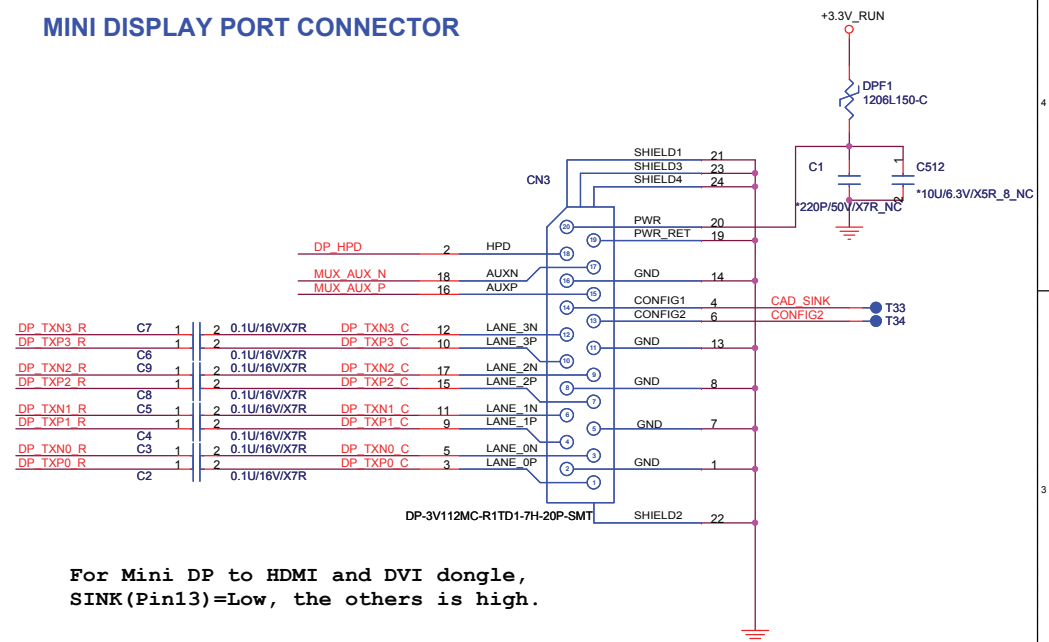
HDMI CONN

<http://hobi-elektronika.net>

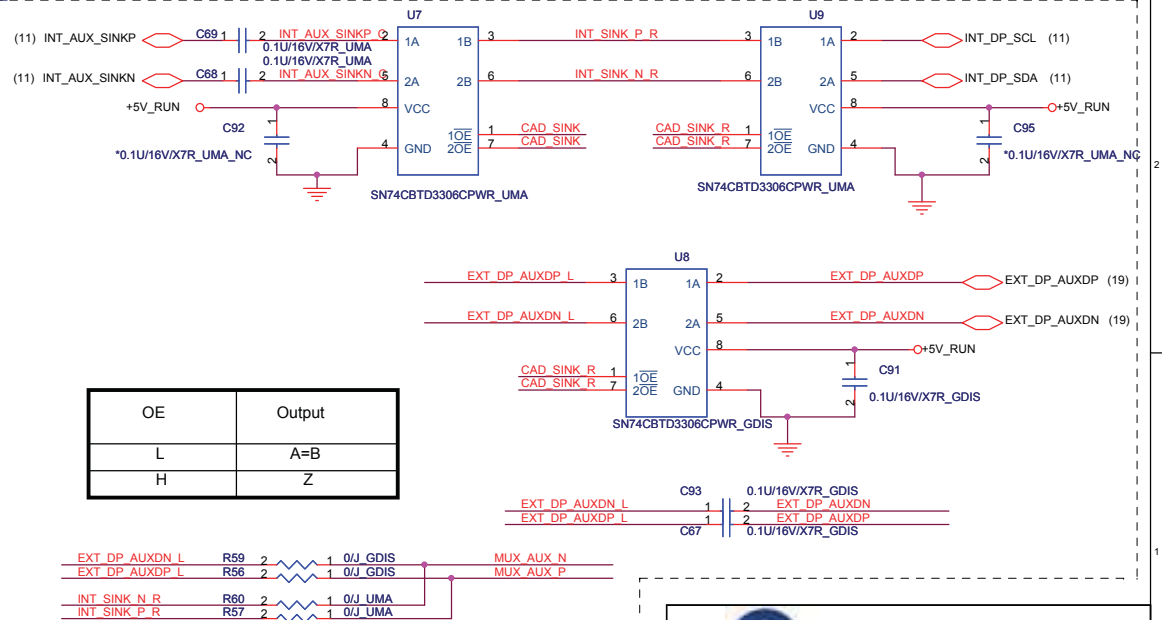
DISPLAY PORT Re-driver



MINI DISPLAY PORT CONNECTOR



For Mini DP to HDMI and DVI dongle,
SINK(Pin13)=Low, the others is high.



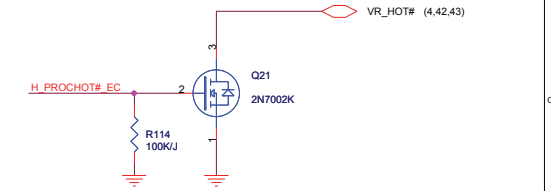
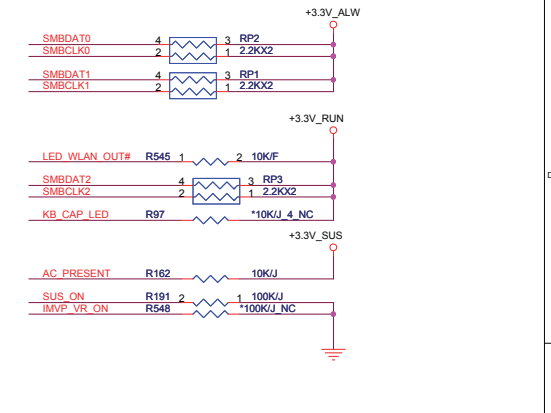
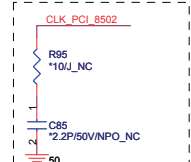
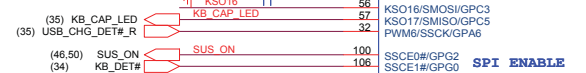
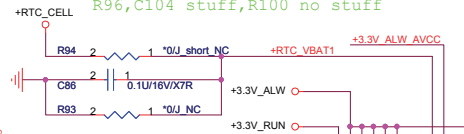
OE	Output
L	A=B
H	Z



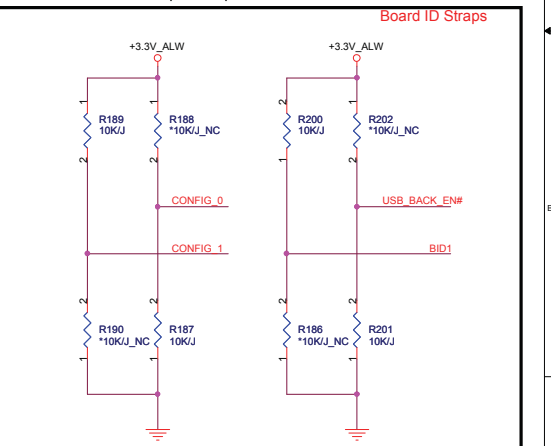
Quanta Computer Inc.

PROJECT : GM6C MLK DIS


MINI DP CONN



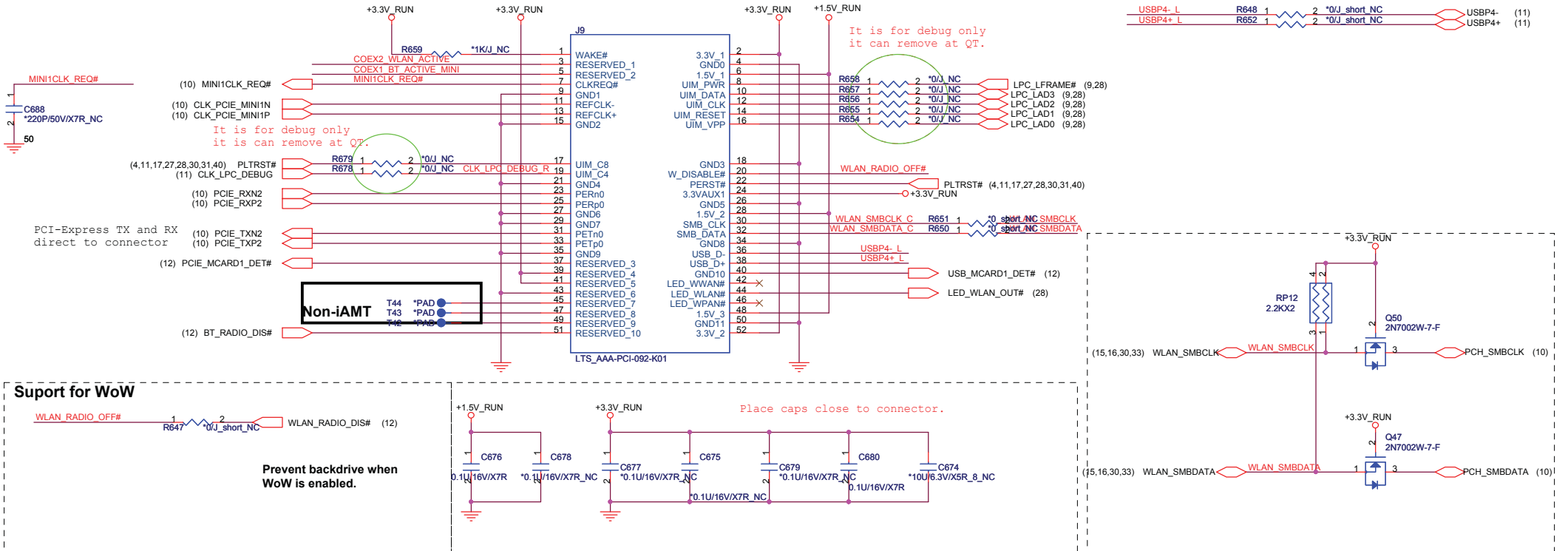
prochot pin level shift



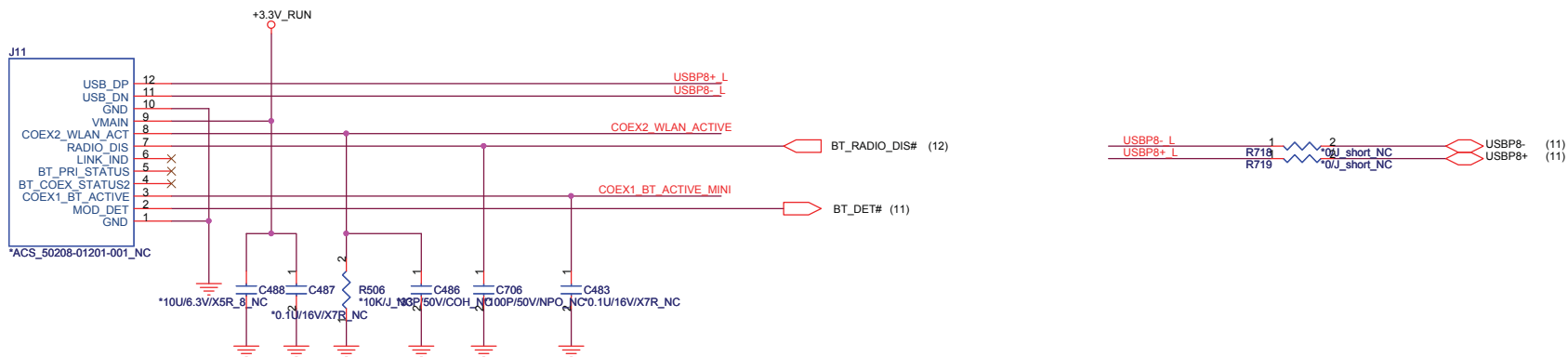
Config 0	Config 1	GM6/GM6C
0	0	UMA
0	1	Optimum-GE
1	0	Studio Discrete
1	1	Optimum-GS

 Quanta Computer Inc. PROJECT : GM6C MLK DIS	
Size	Document Number SIO (ITE8518)
Date: Friday, January 07, 2011	Sheet 28 of 59

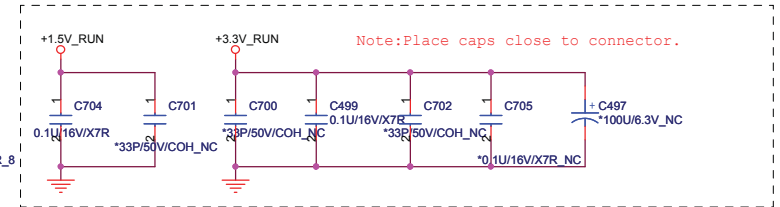
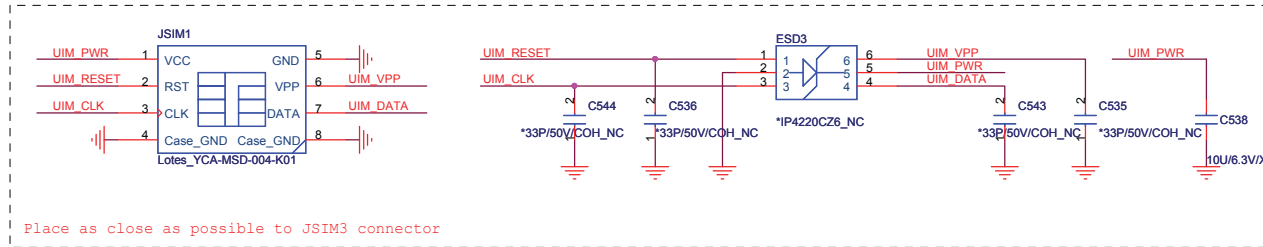
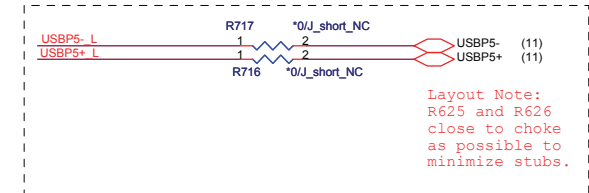
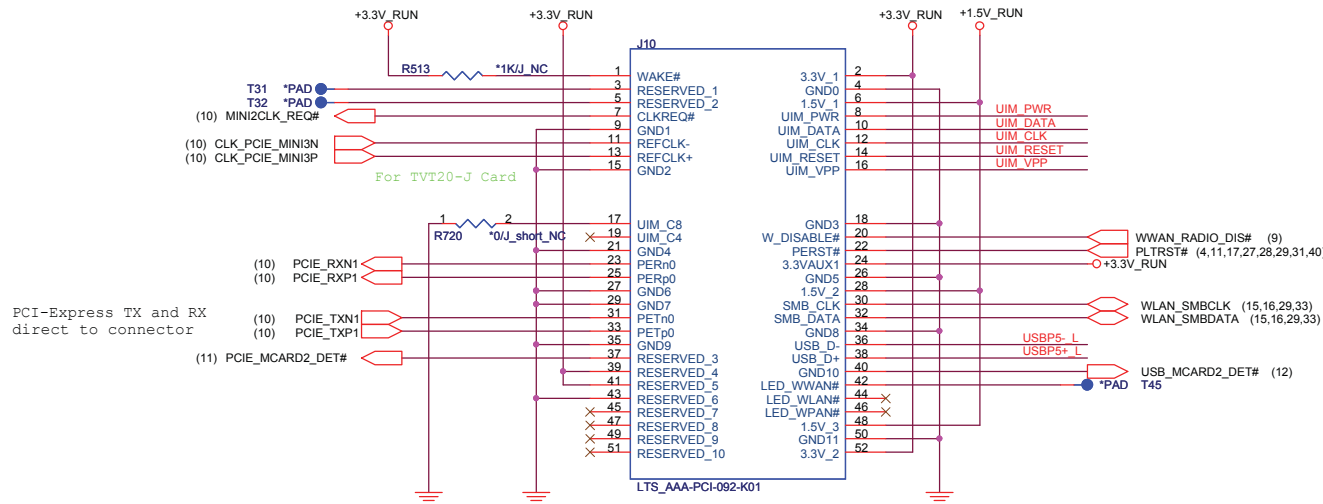
MiniCard WLAN connector

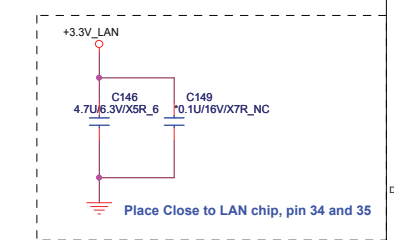
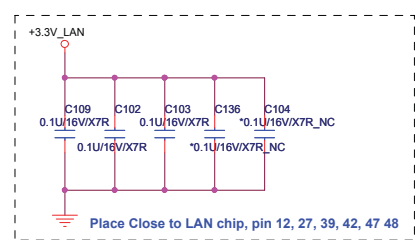
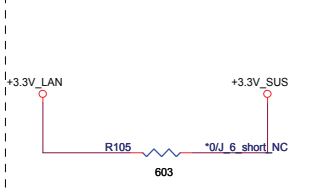
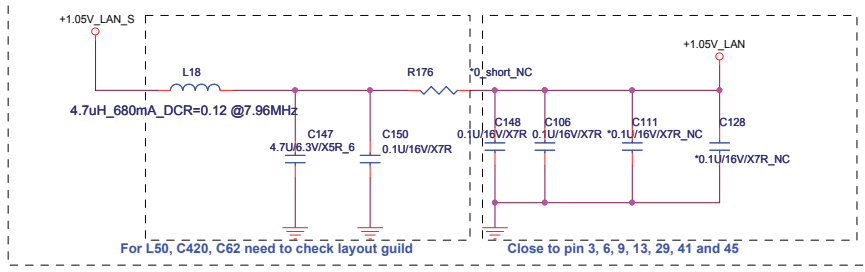


Support Dell BT375 (Little Stone) module (XPS) W TO B

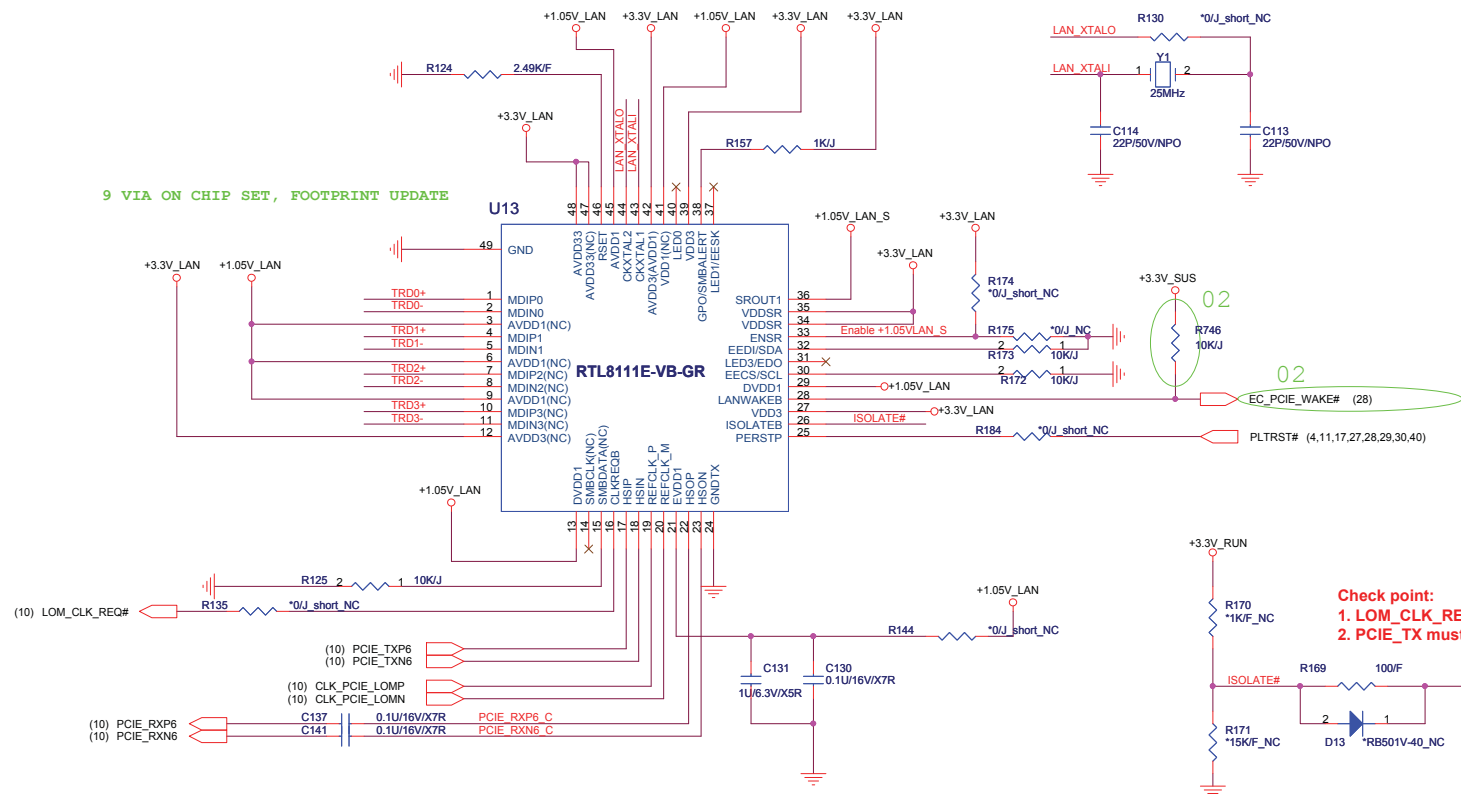


MiniCard WWAN connector

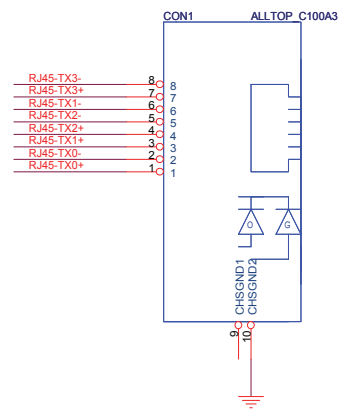




9 VIA ON CHIP SET, FOOTPRINT UPDATE



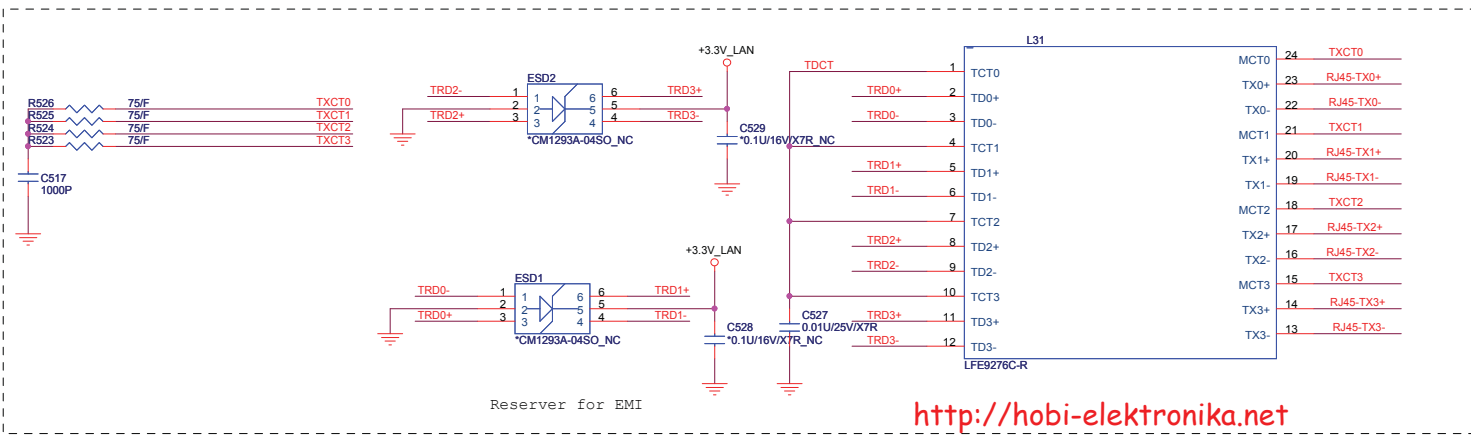
RJ-45 Connector



Wait for Connector list to update

Check point:
1. LOM_CLK_REQ# and PCIE_WAKE# needs to be pull up by PCH side
2. PCIE_TX must have AC cap at PCH side

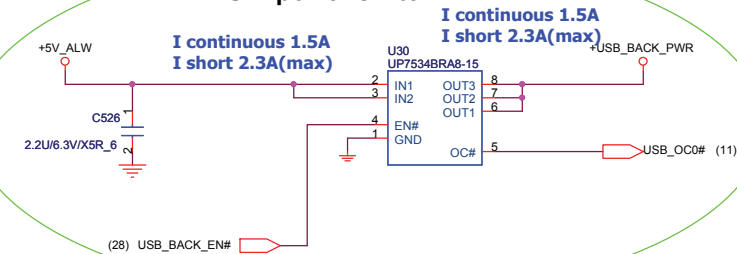
Isolate# is for power saving.
It needs to pull low when system state in S3, S4, and S5.
pull high when system at S0 state



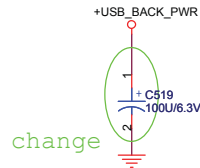
<http://hobi-elektronika.net>

ESATA + USB Conn + Power Share

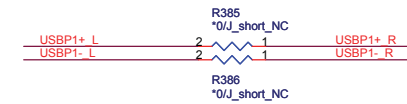
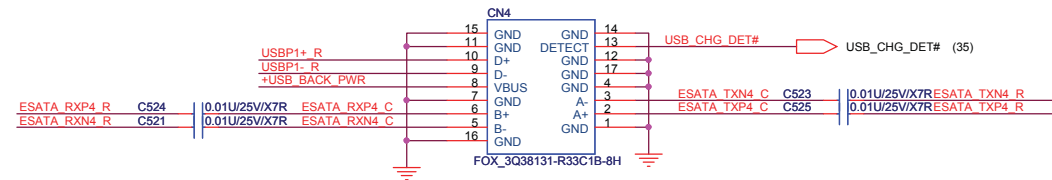
UPI power switch



USB_BACK_EN# needs to be low when system S3 and S5 for USB charge

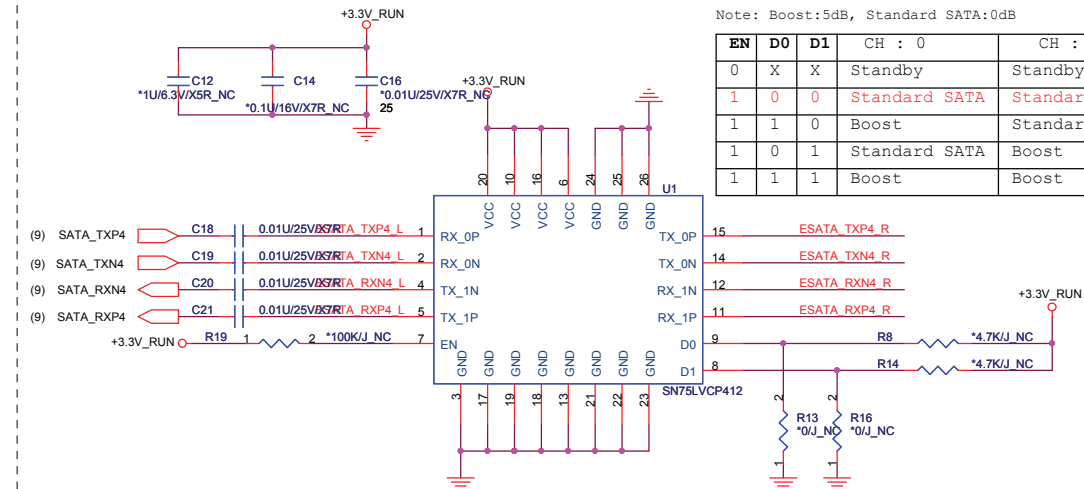


This pin connects to 3VALW ON POWER LOGIC



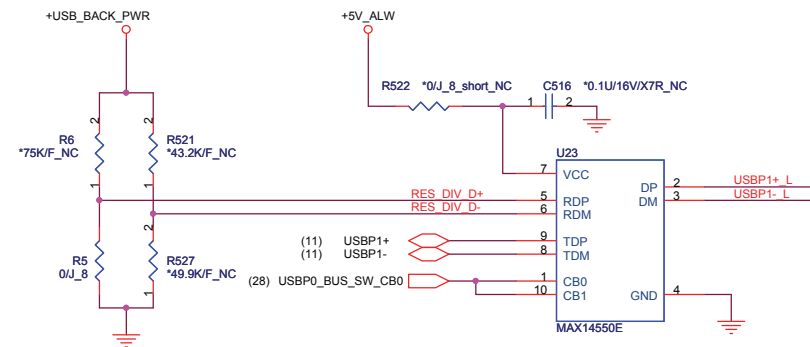
E-SATA Re-driver

Layout Note: Please put those on the same side of MB PCB



Note: Boost:5dB, Standard SATA:0dB

EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost



EC needs to drive CB0/CB1 pins to low when system S3/S5 and drive high when system S0.

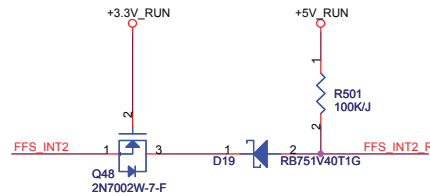
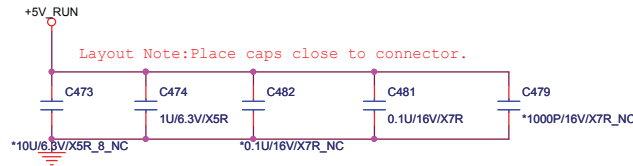
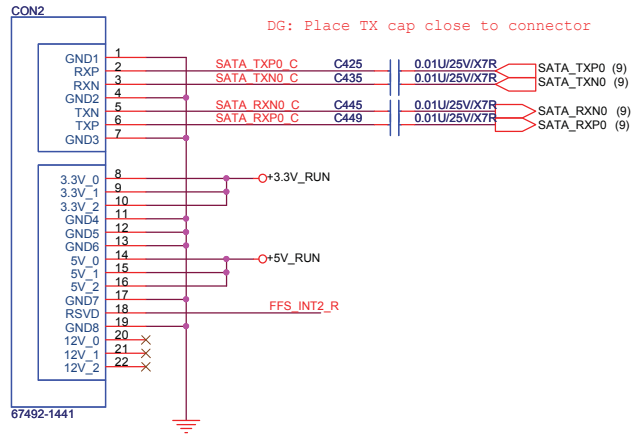
U49 PN and Footprint needs to double check

R15 needs to be 49.9K_F if we use external resistors.

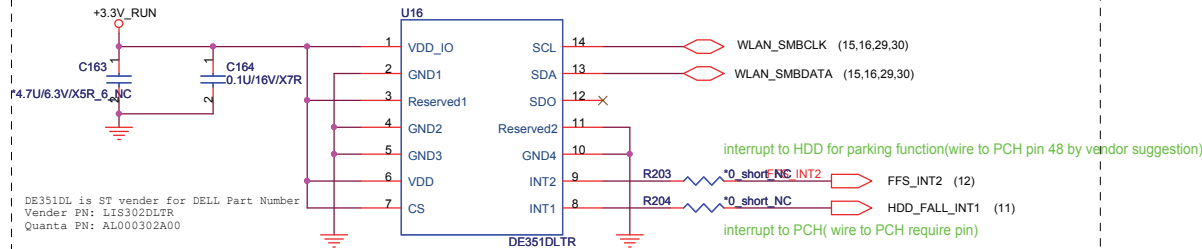
CB0	CB1	Function
0	0	Auto Detection active
1	1	USB Function only

(5V)-43.2K-(D-)-49.9K-GND (about 2.68V)
(5V)-75.0K-(D+)-49.9K-GND (about 2.00V)

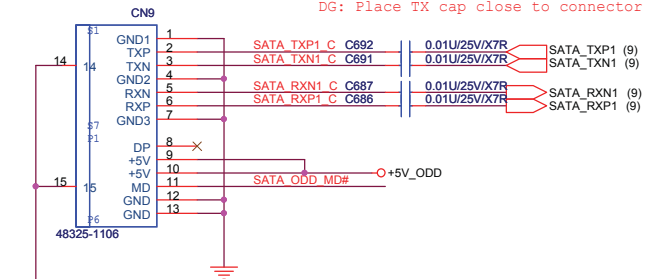
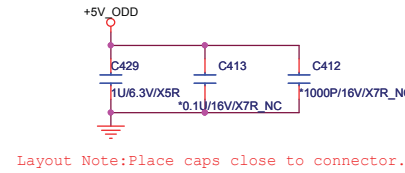
SATA Connector.



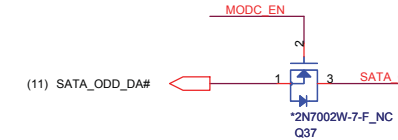
3-axis Fall Sensor (HDD data protector)



ODD Connector



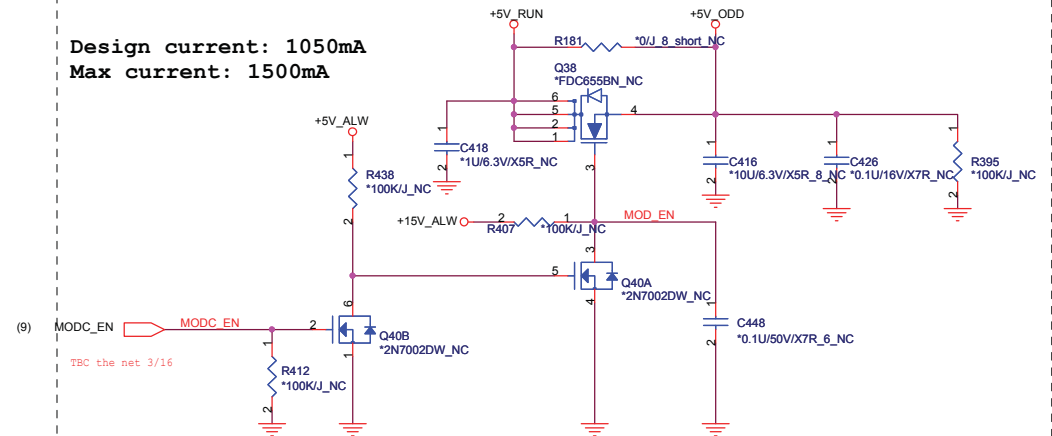
Backwards Compatibility



Drive powered on, MD# is High
Drive powered off, MD# is Low

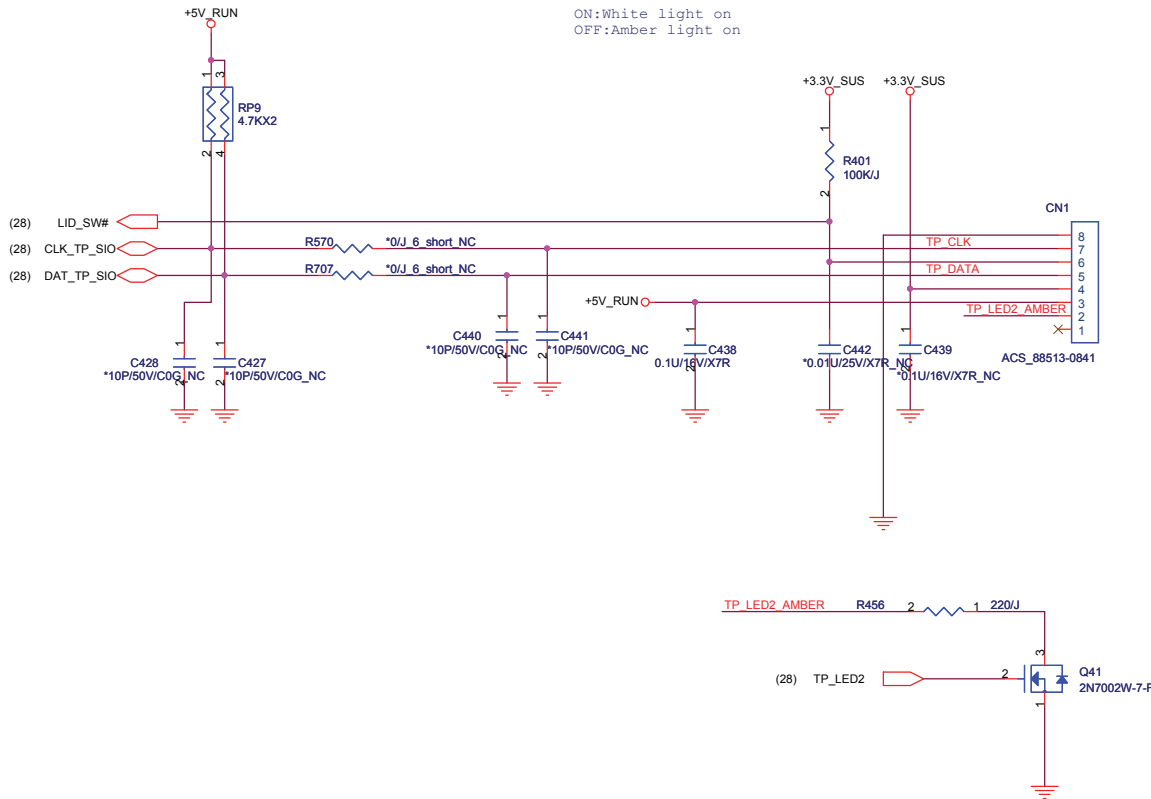
Because the drive does not support ZPODD, the driver never powers off the power FET and never connects the MD/DA pin to the drive

Design current: 1050mA
Max current: 1500mA

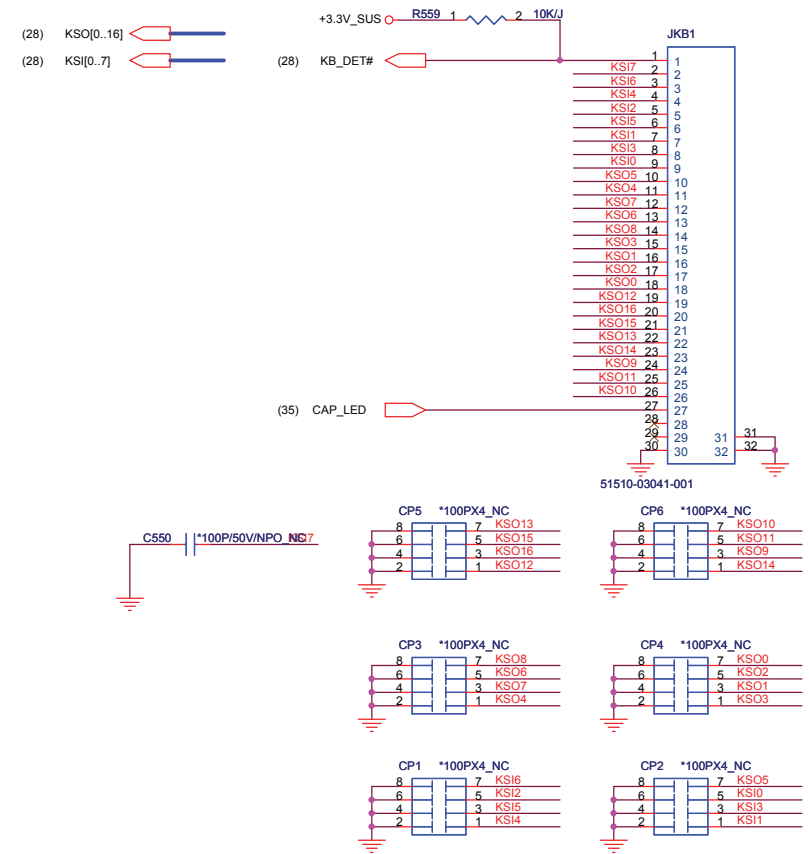


Touch Pad

ON:White light on
OFF:Amber light on



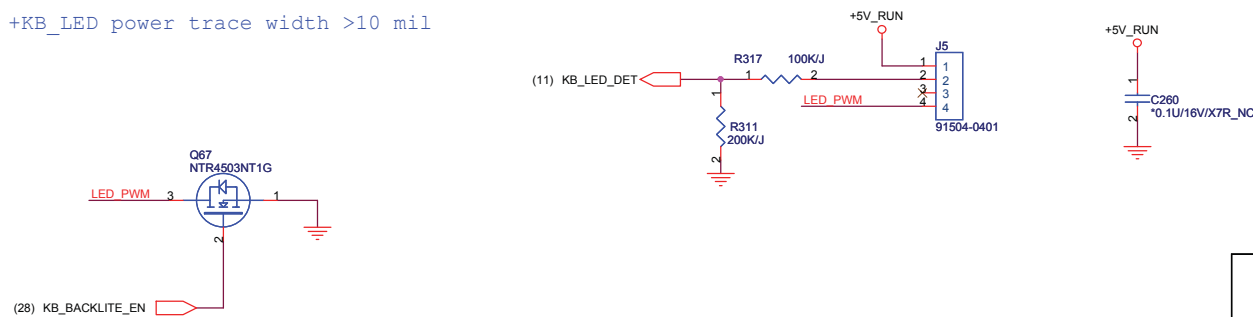
KEYBOARD CONNECTOR



Layout Note: 100P CAPS CLOSE TO JKB3

Key board illumination

+KB_LED power trace width >10 mil



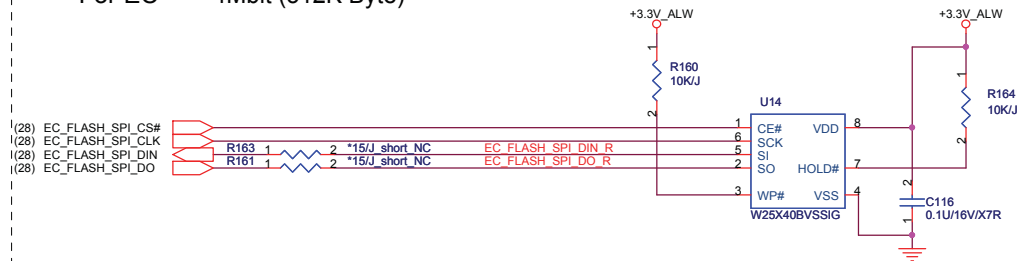
Quanta Computer Inc.

PROJECT : GM6C MLK DIS

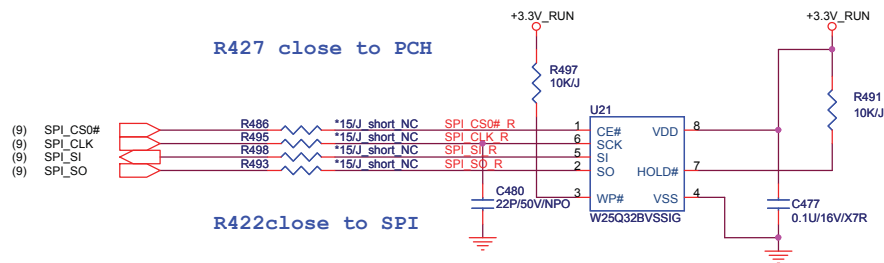
Size	Document Number	Rev
	TP/KB	1A
Date:	Friday, January 07, 2011	Sheet 34 of 59

<http://hobi-elektronika.net>

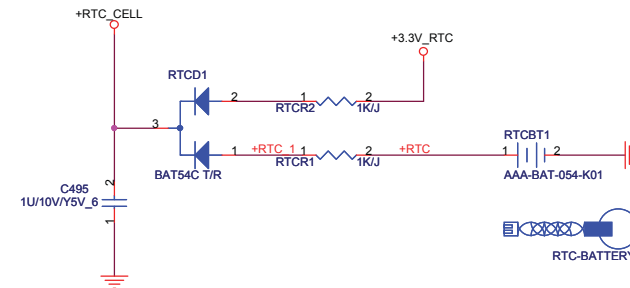
For EC 4Mbit (512K Byte)



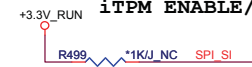
For PCH 32Mbit (4M Byte)



RTC BATTERY



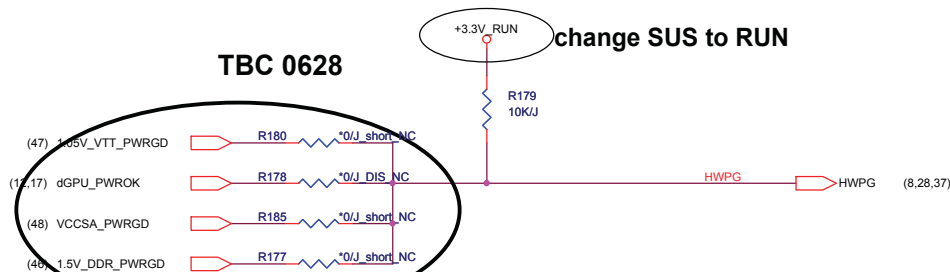
iTPM ENABLE/DISABLE



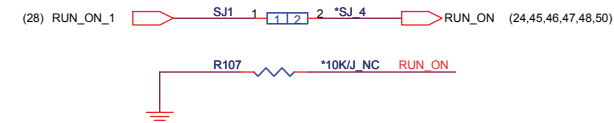
TPM Function	R428
Enable	Mount
Disable	NC (Default)

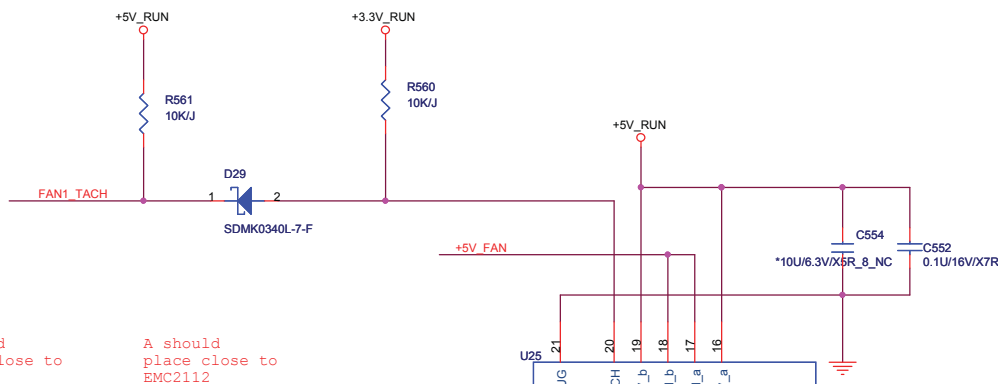
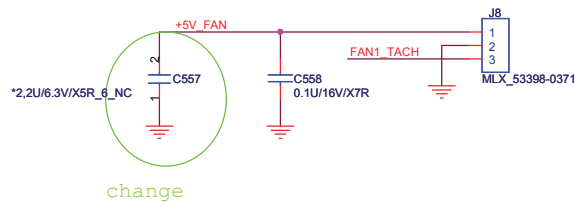
RESET CIRCUIT

TBC 0628



delet VTT_POWERGOOD(07/12)





Need to check with BIOS

ADDR_SEL

HIGH: 0101 110xb

OPN: 0111 101xb

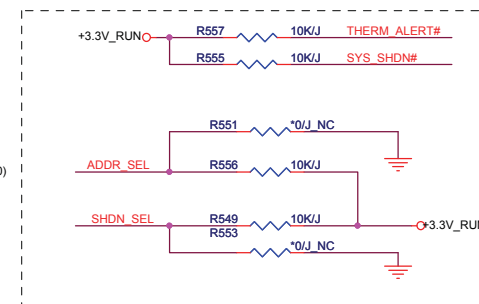
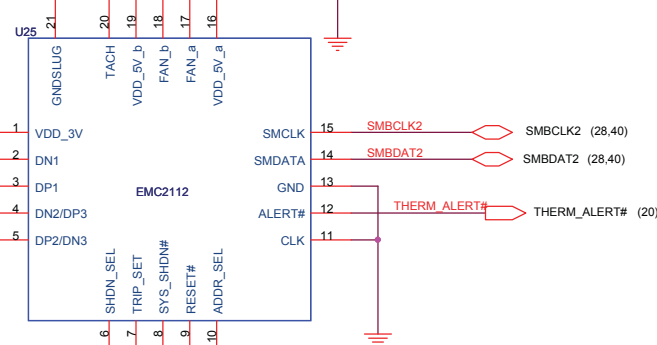
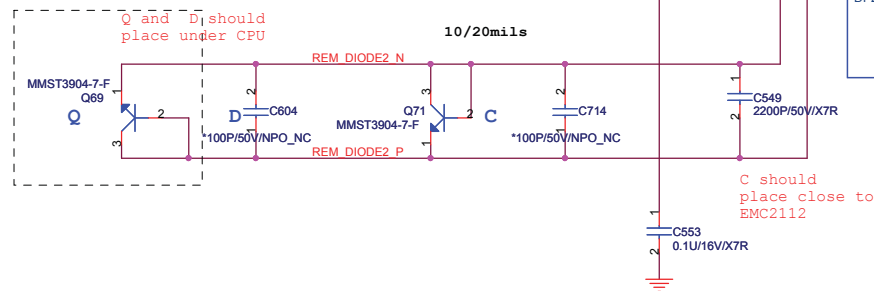
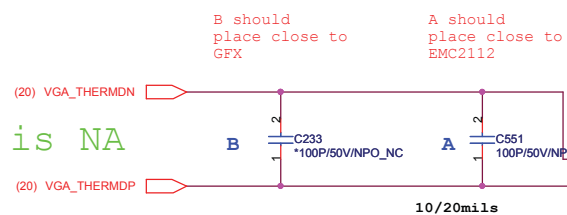
GND: 0101 111xb

SHDN_SEL

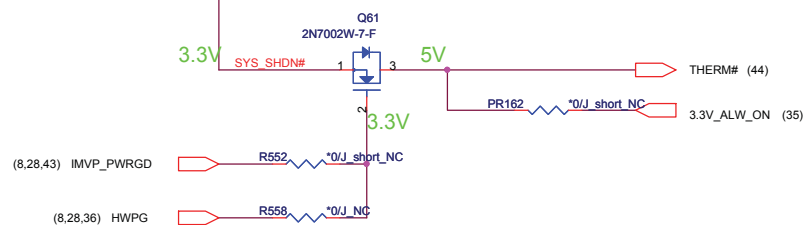
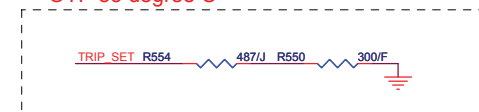
HIGH: External Diode 2 Mode

OPN: AMD CPU/Diode Mode

GND: Intel Transistor Mode

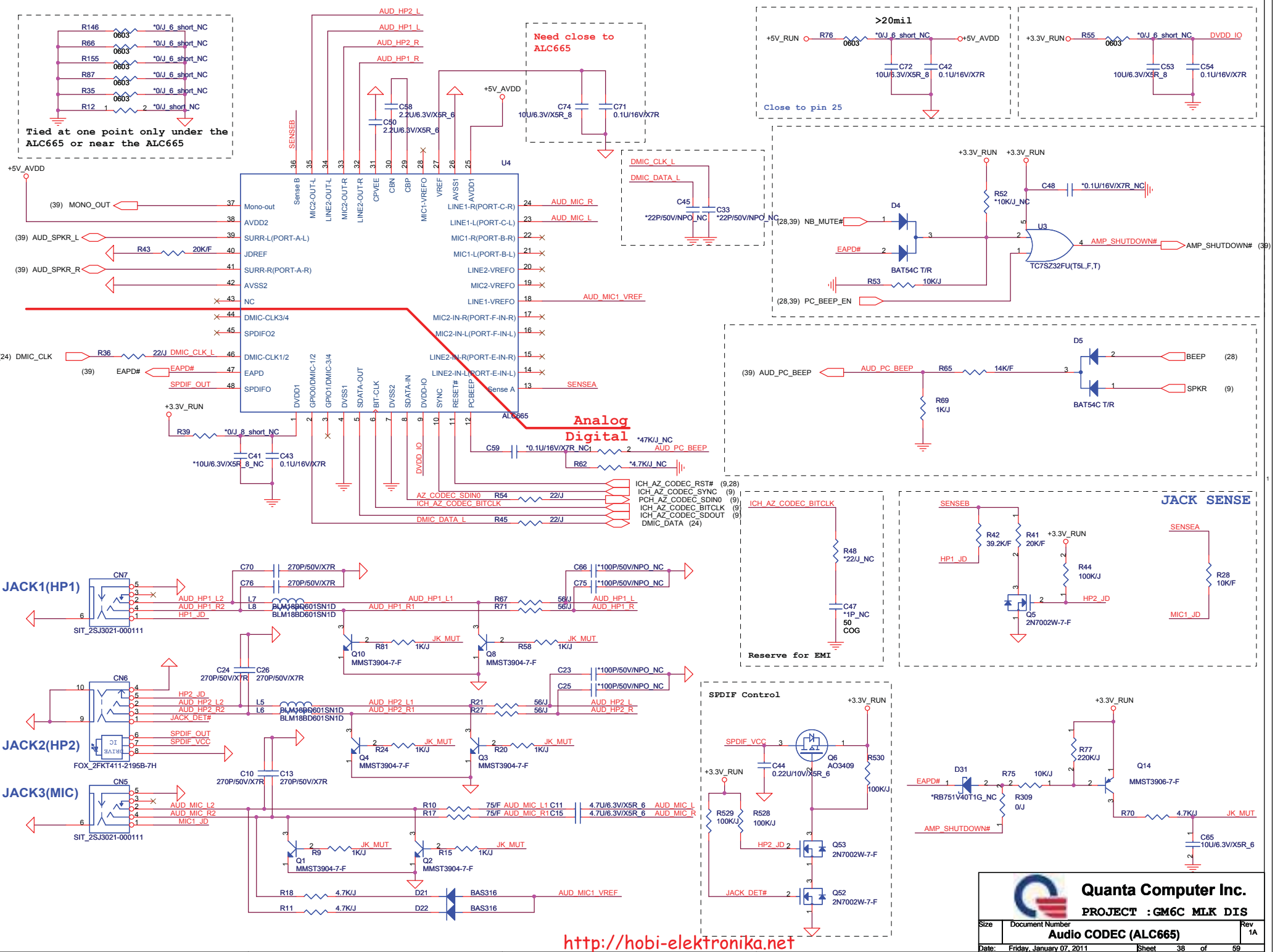


OTP 85 degree C



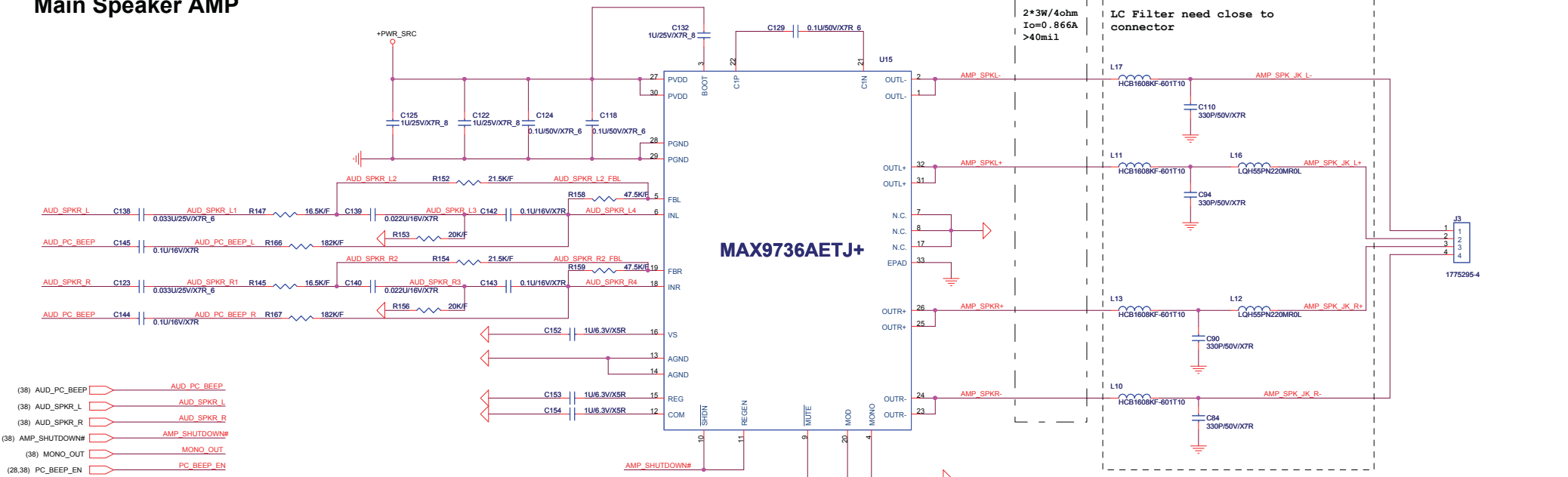
reserve HWPG only HW control (07/12)

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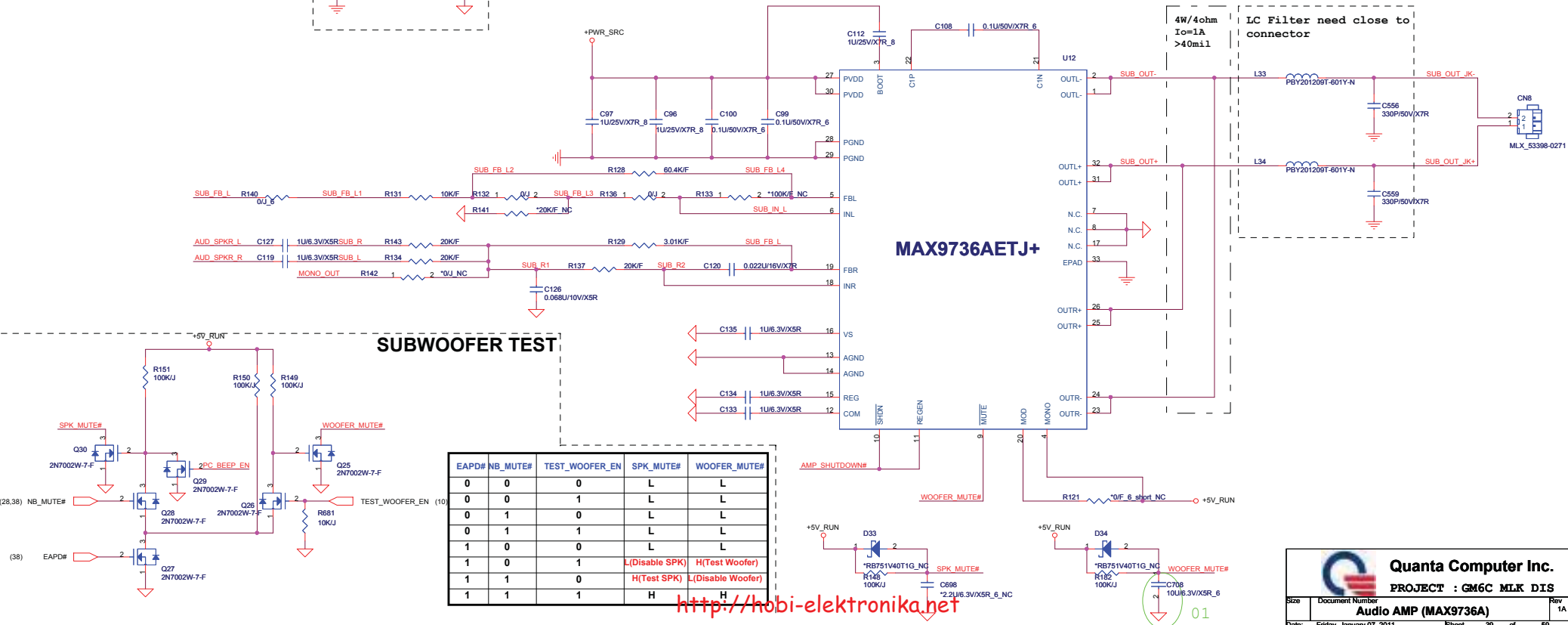


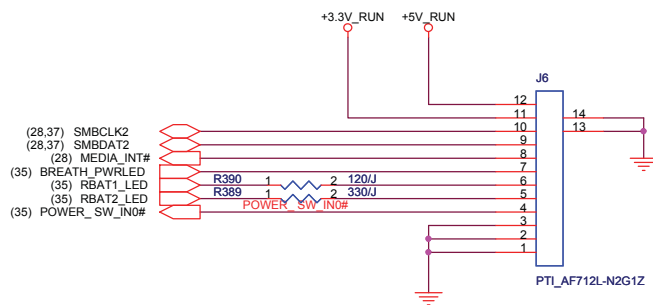
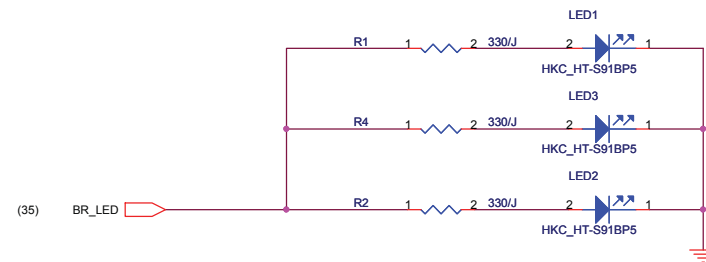
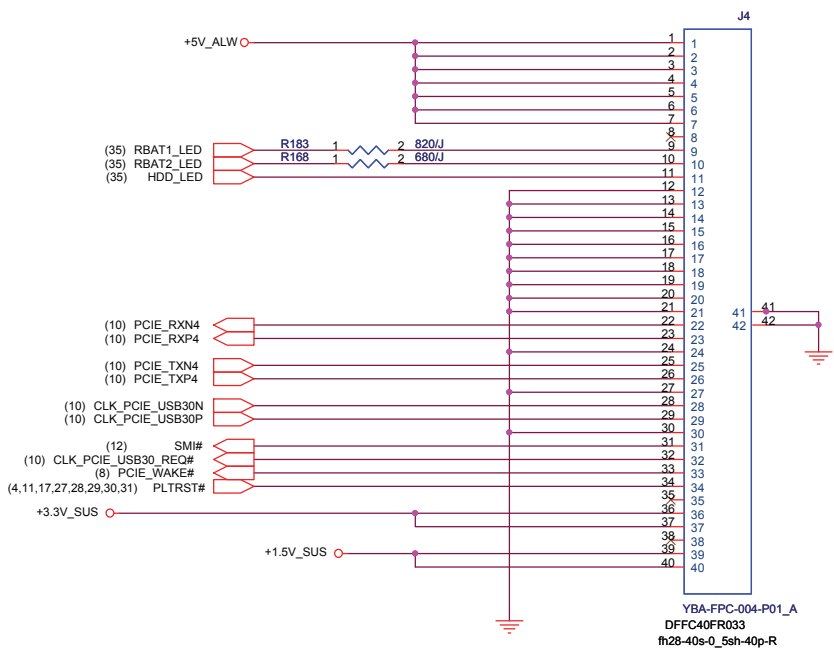
<http://hobi-elektronika.net>

Main Speaker AMP



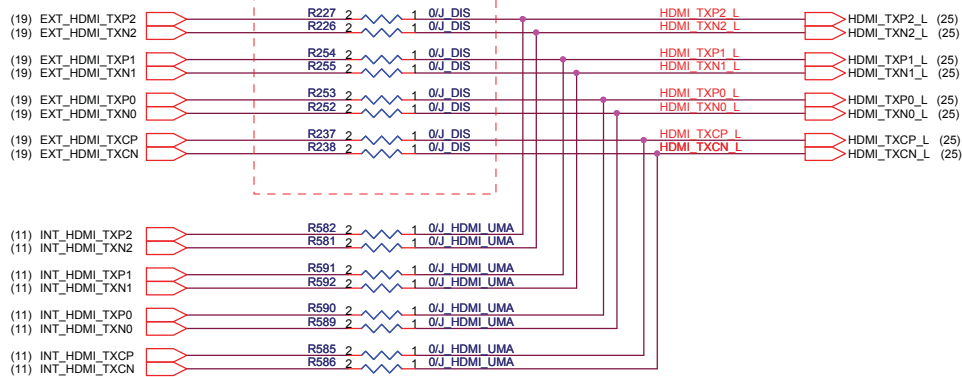
SUBWOOFER AMP



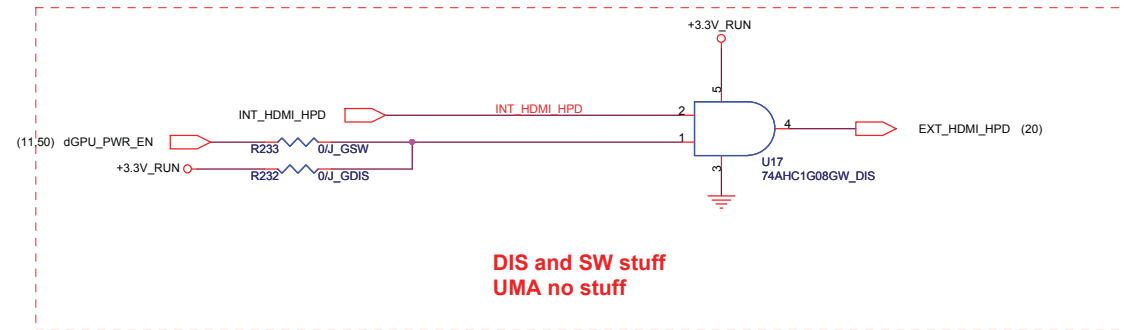
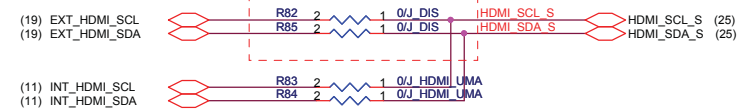


HDMI Switch

DIS and SW stuff
UMA no stuff

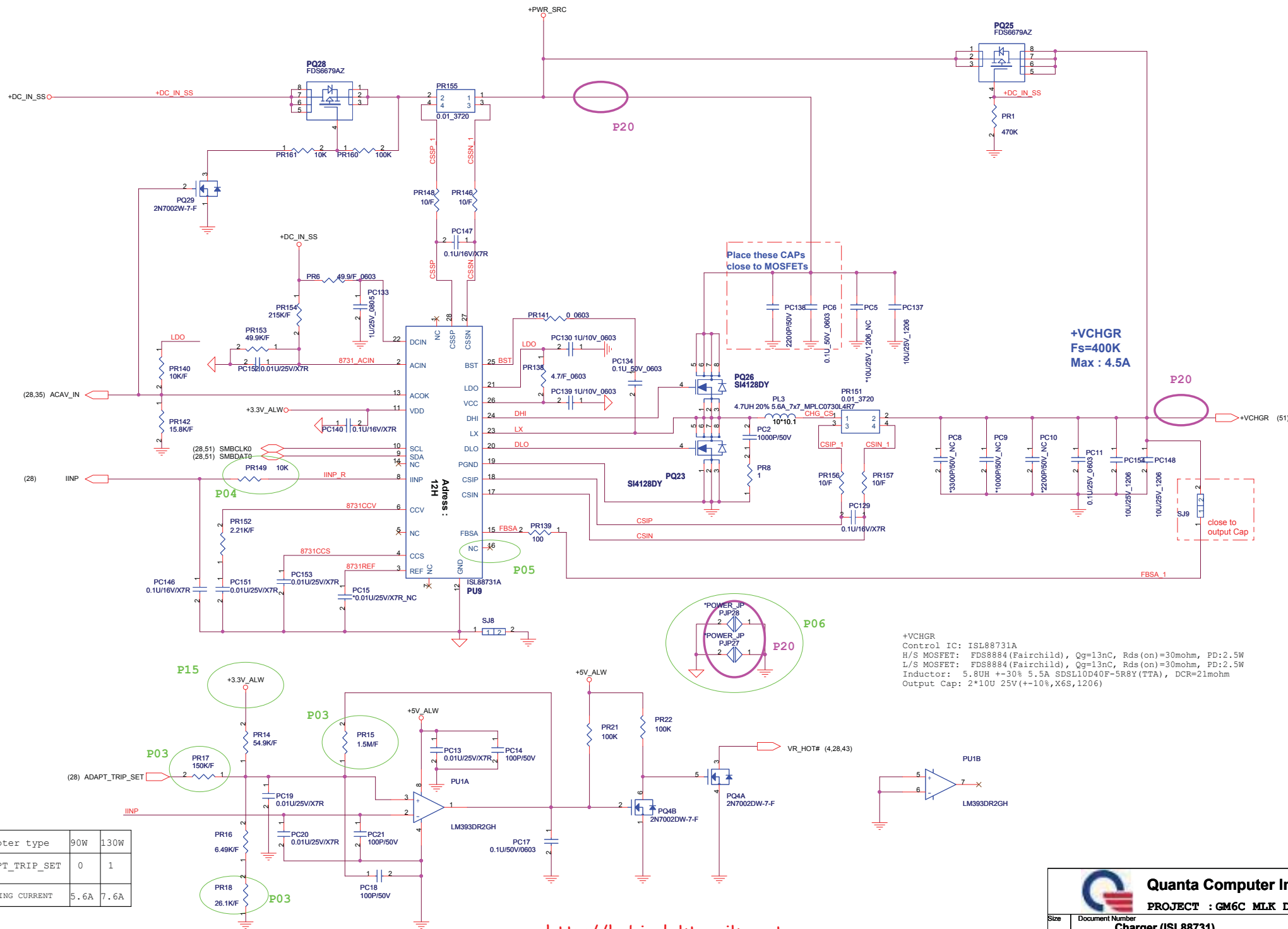


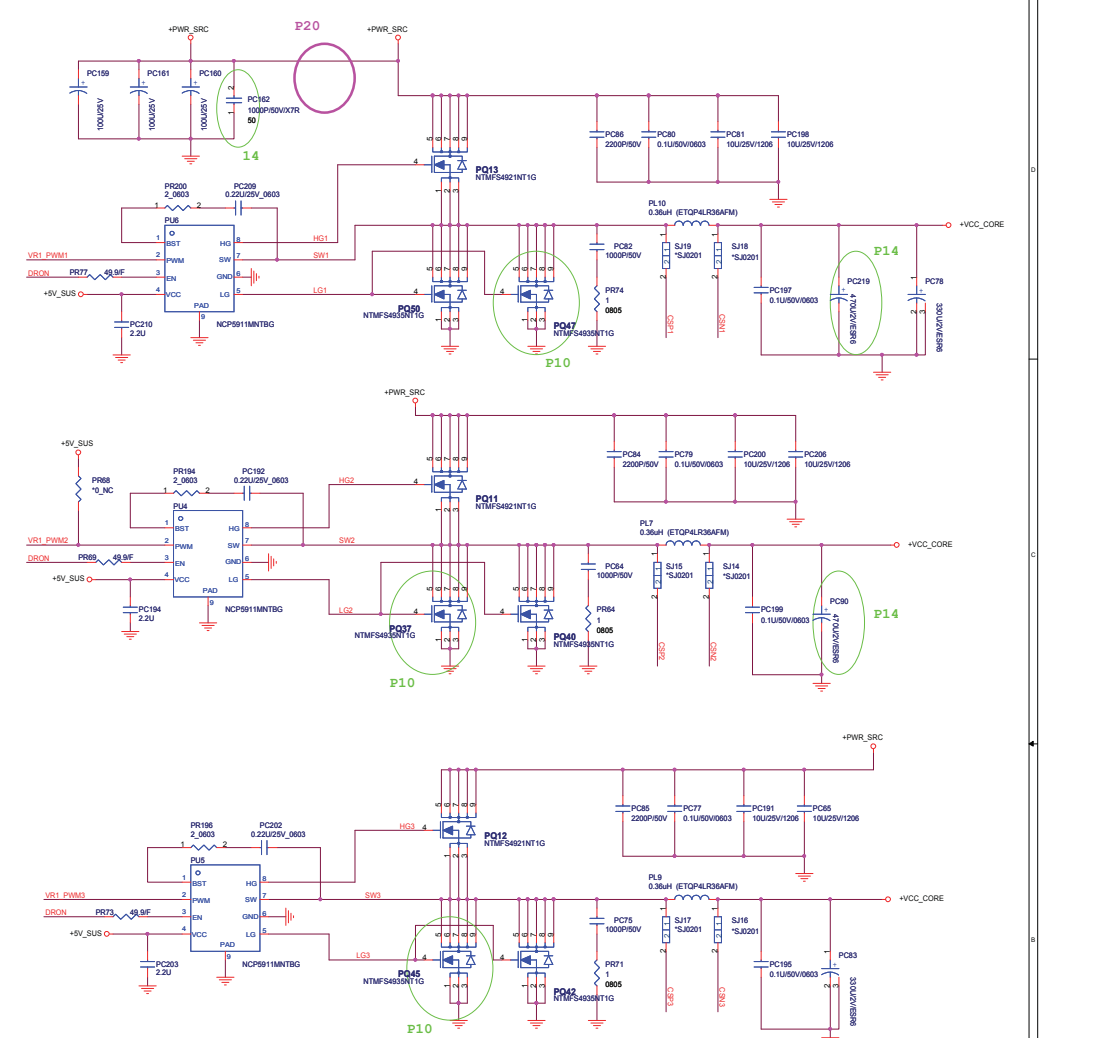
DIS and SW stuff
UMA no stuff



DIS and SW stuff
UMA no stuff








IGPU Power

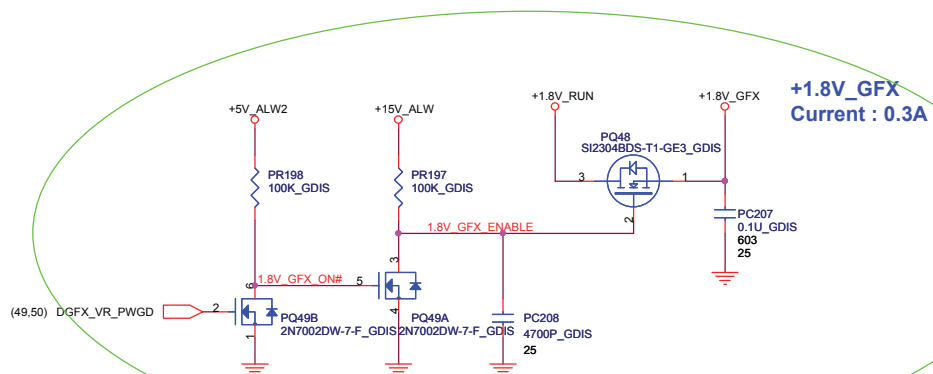
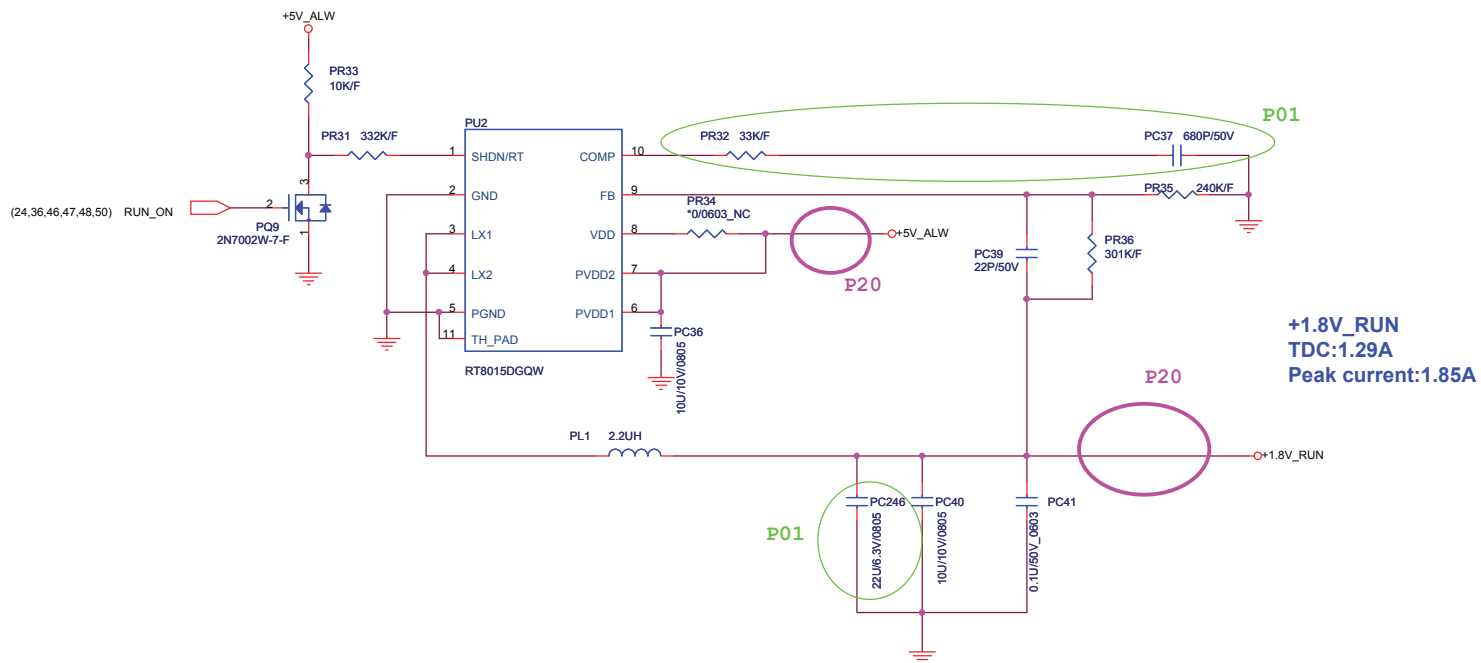
The schematic diagram illustrates the power distribution for the IGPU. It shows the connection of various power planes (P20, P12, P13) to the PWR_SRC and VCC_IGPU_CORE. Key components include capacitors (PC187, PC186, PC185, PC184, PC190, PC180), inductors (P187, P185, P184), and various power planes (P20, P12, P13). The diagram is labeled "IGPU Power".

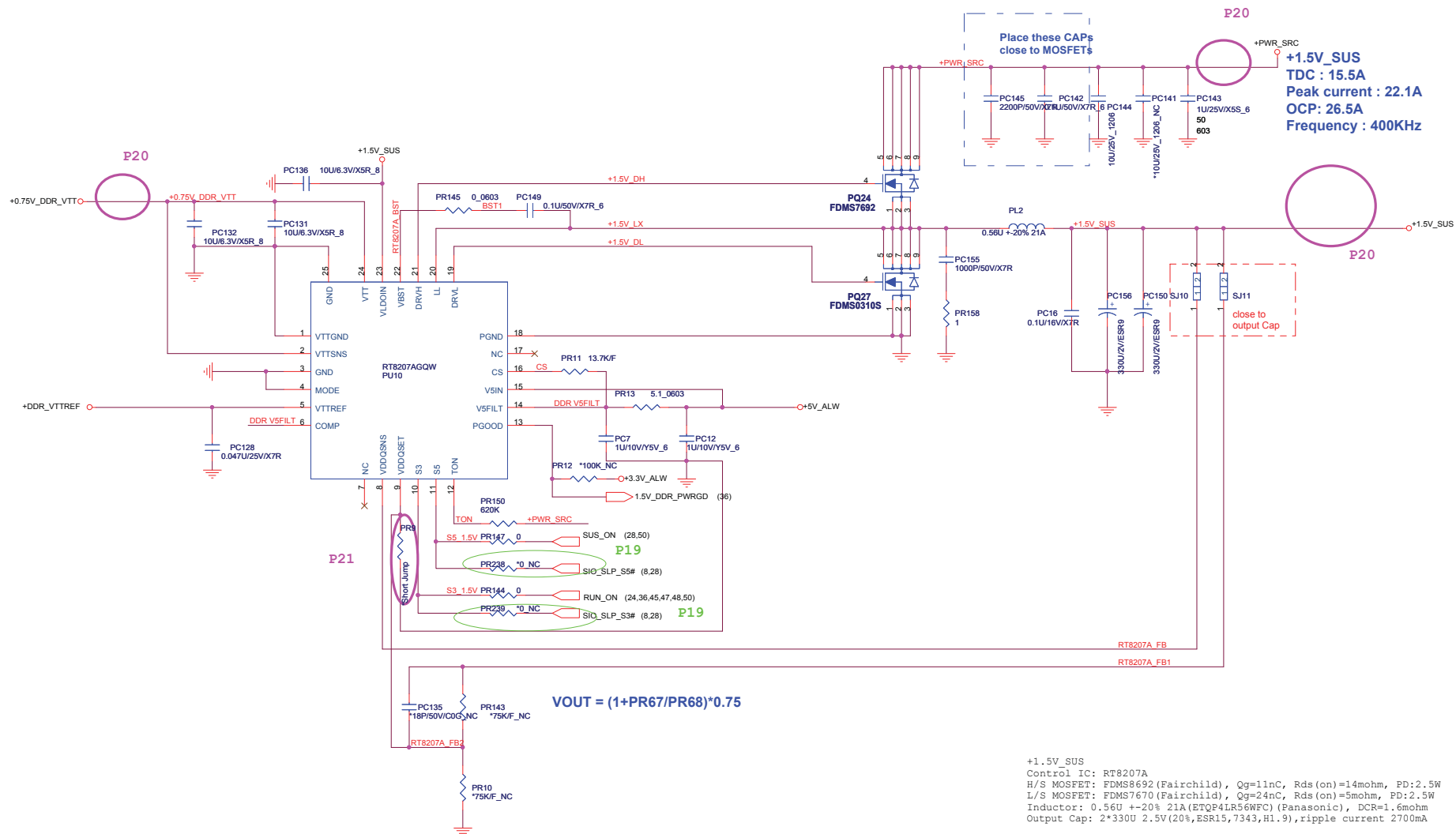
	UMA	Optimus
PC180, C612	470uF CH747RM8800	330uF CH733RM8831



Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
		1





VDDQ and VTT discharge control

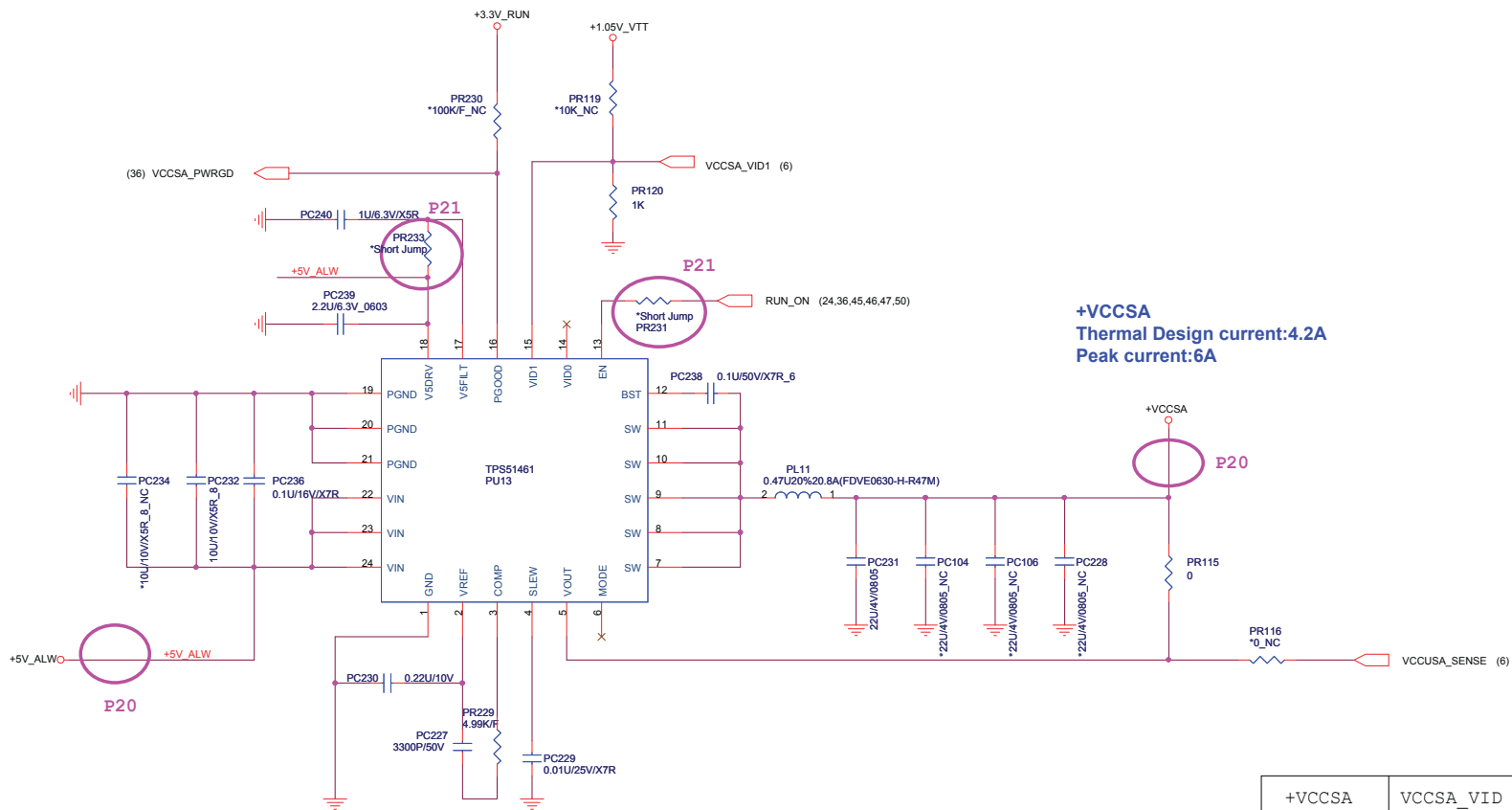
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)



+VCCSA	VCCSA_VID
0.8V	High
0.9V	Low

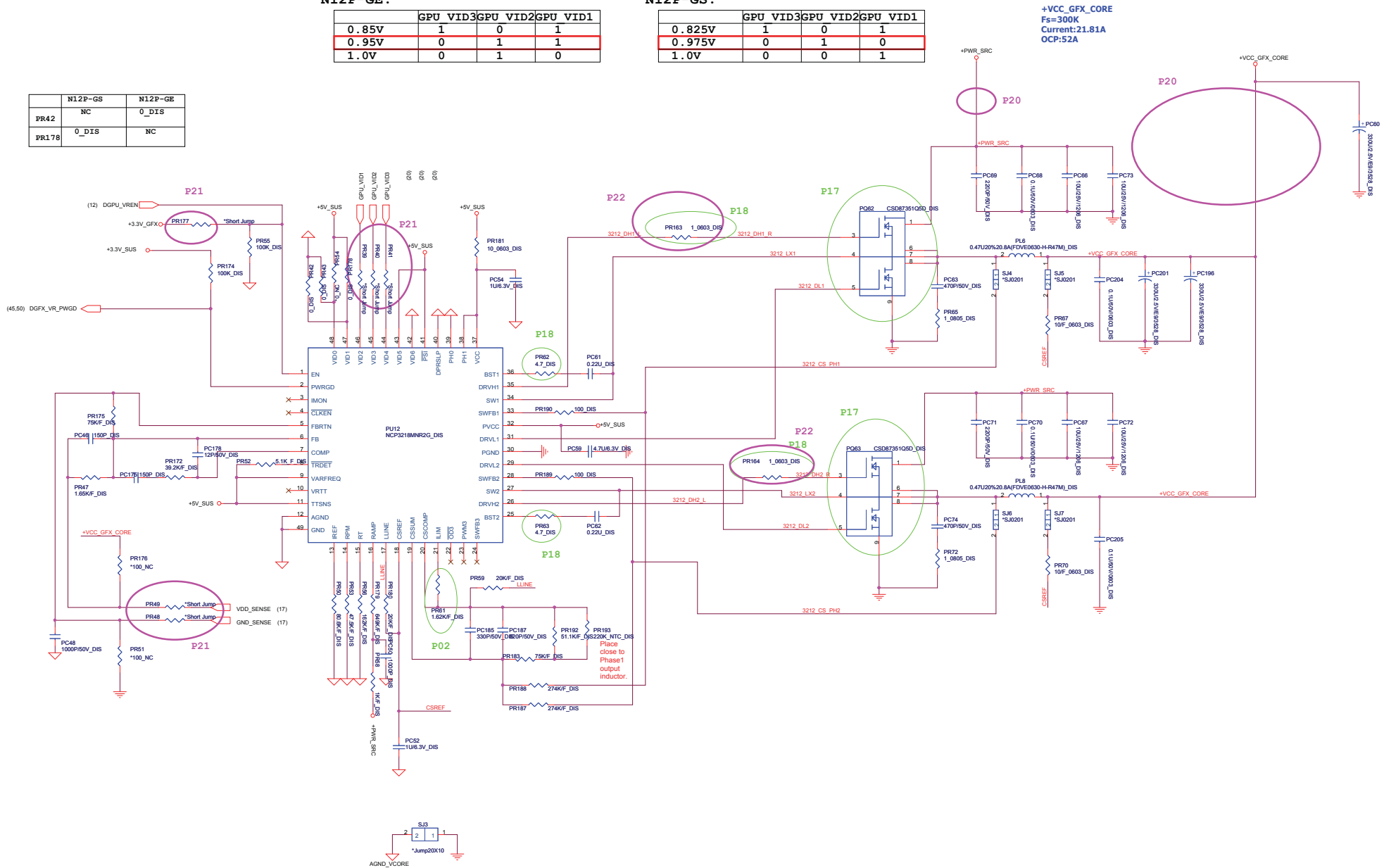
N12P-GE:

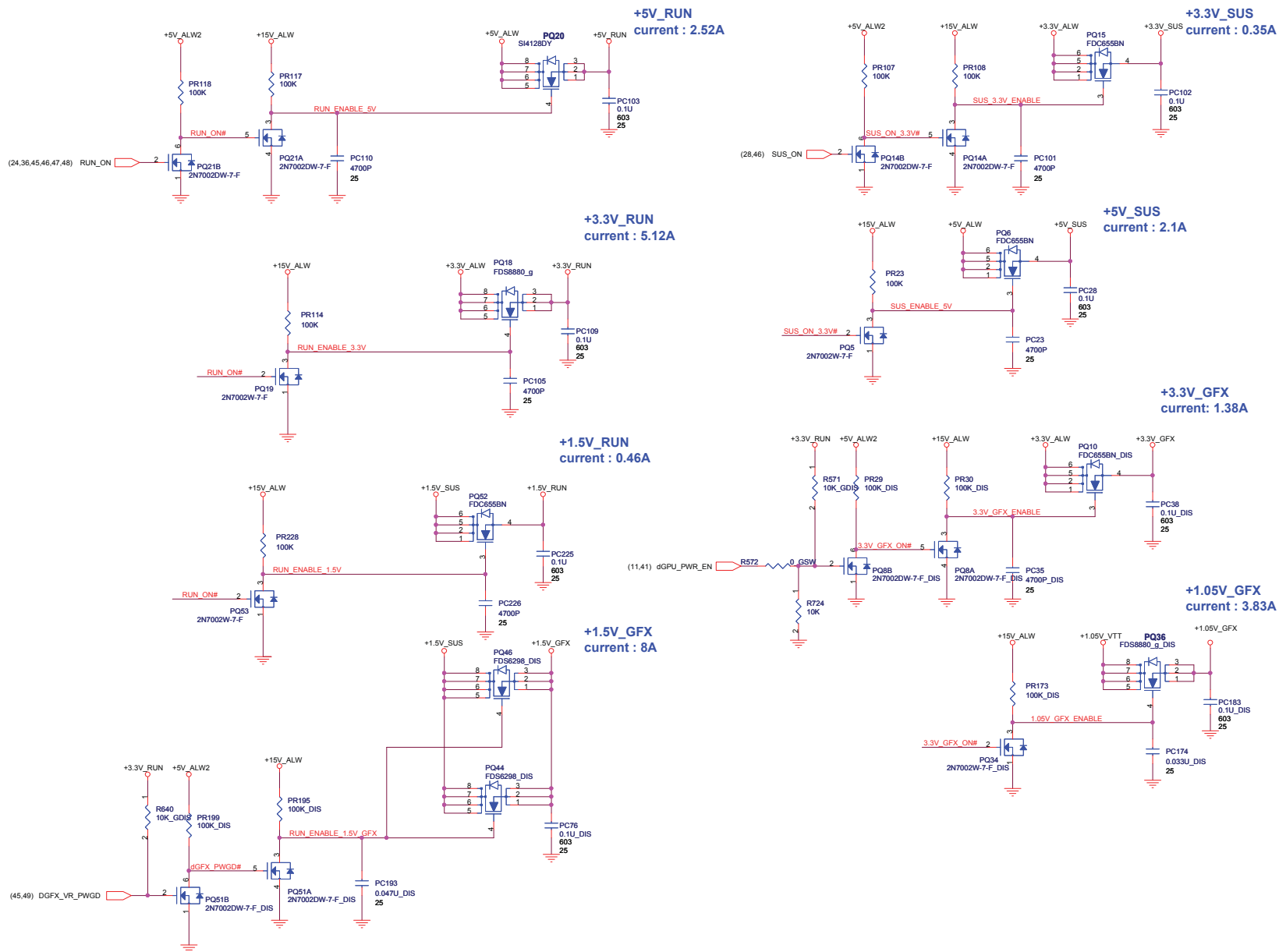
GPU VID3	GPU VID2	GPU VID1
0.85V	1	0
0.95V	0	1
1.0V	0	0

N12P-GS:

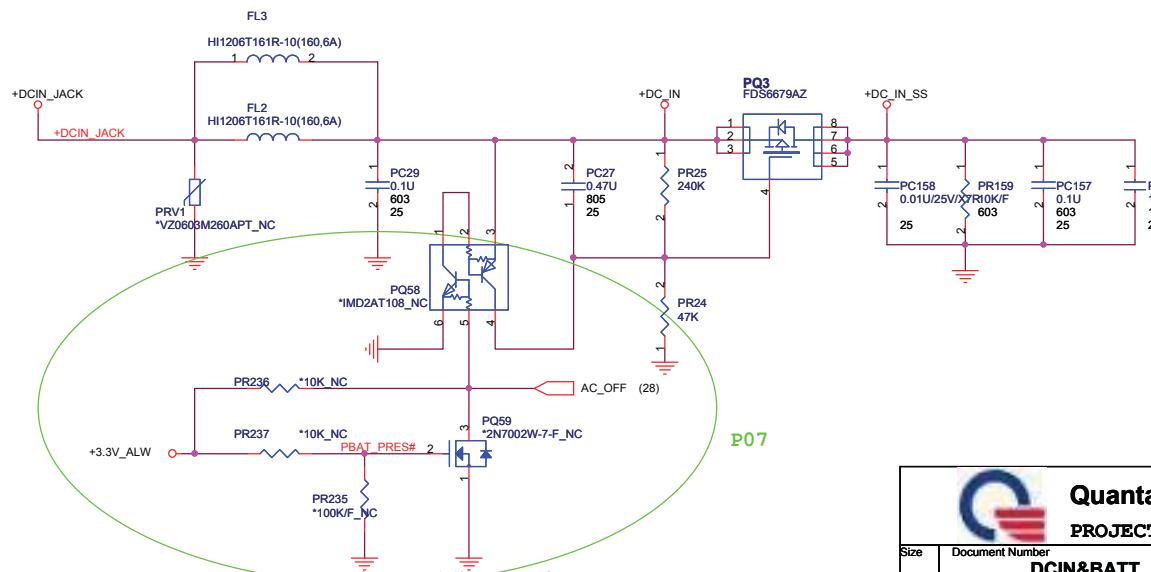
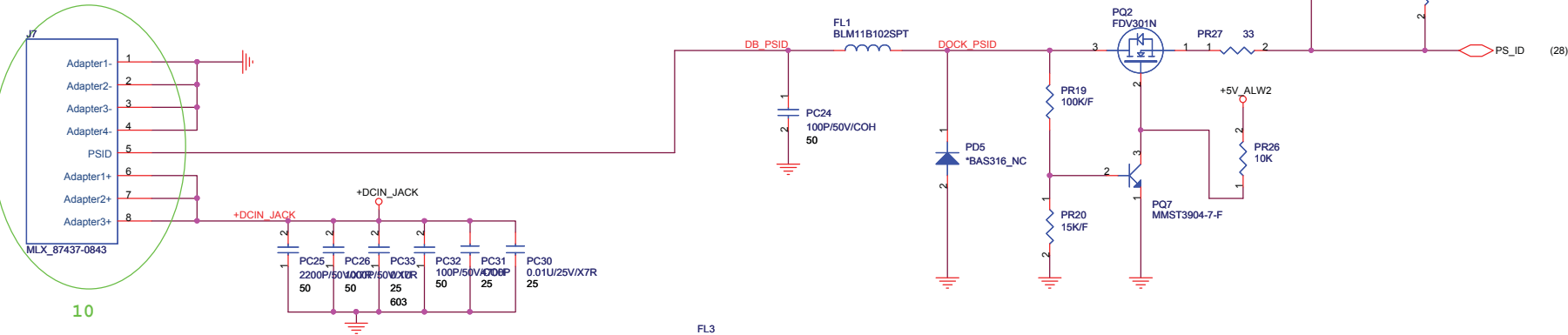
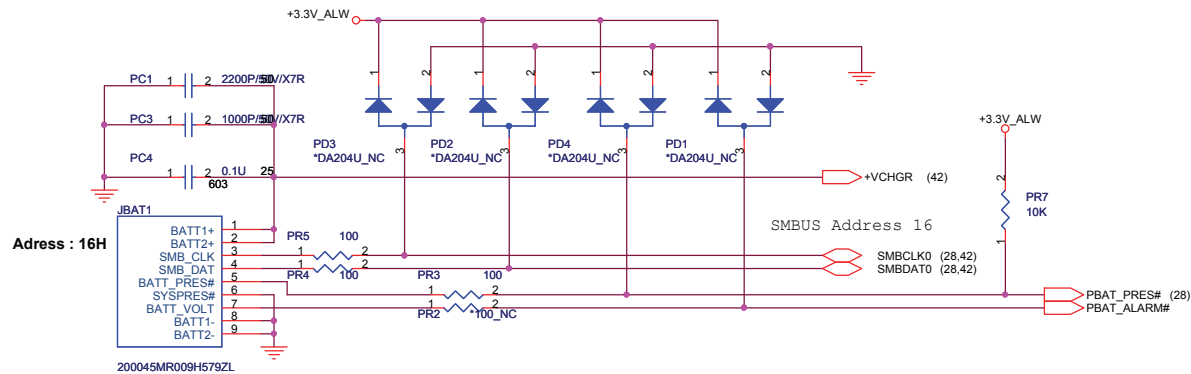
GPU VID3	GPU VID2	GPU VID1
0.825V	1	0
0.975V	0	1
1.0V	0	0

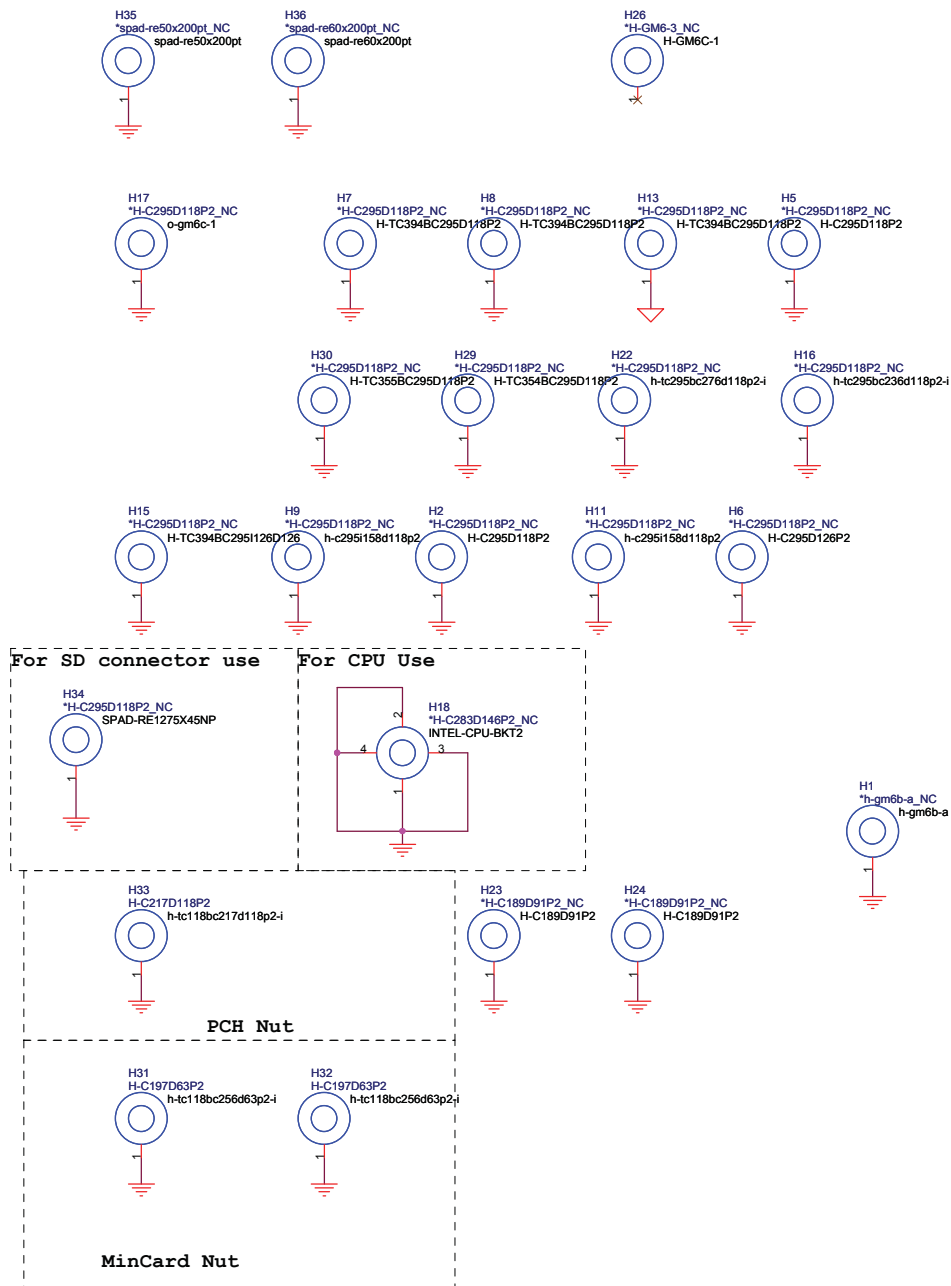
	N12P-GS	N12P-GE
PR42	NC	0_DIS
PR178	0_DIS	NC

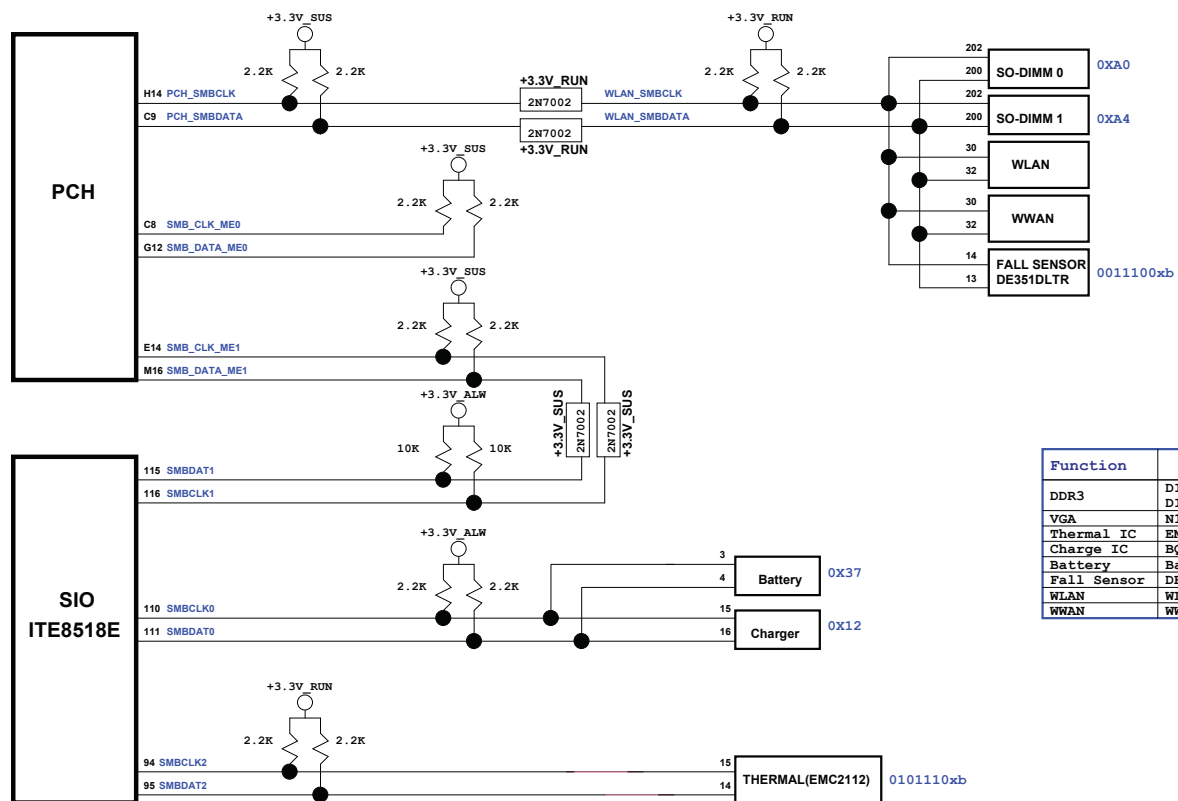




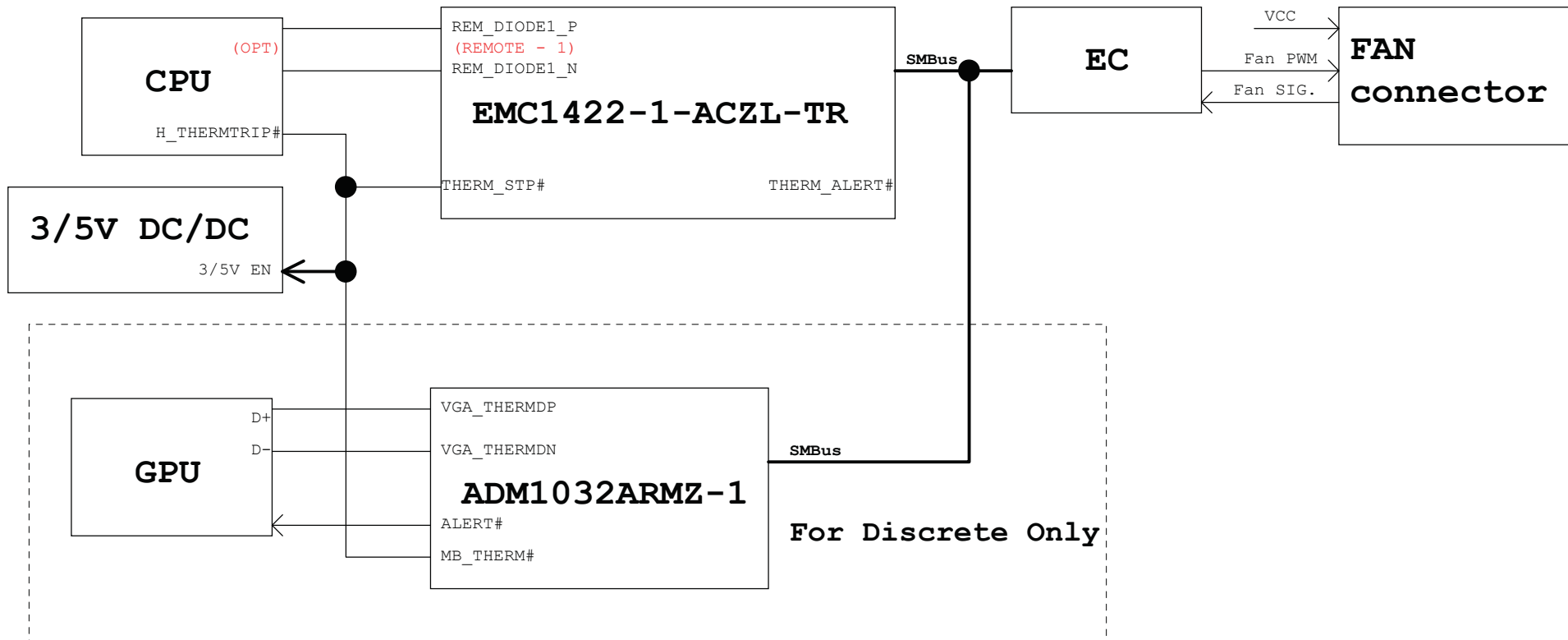
<http://hobi-elektronika.net>

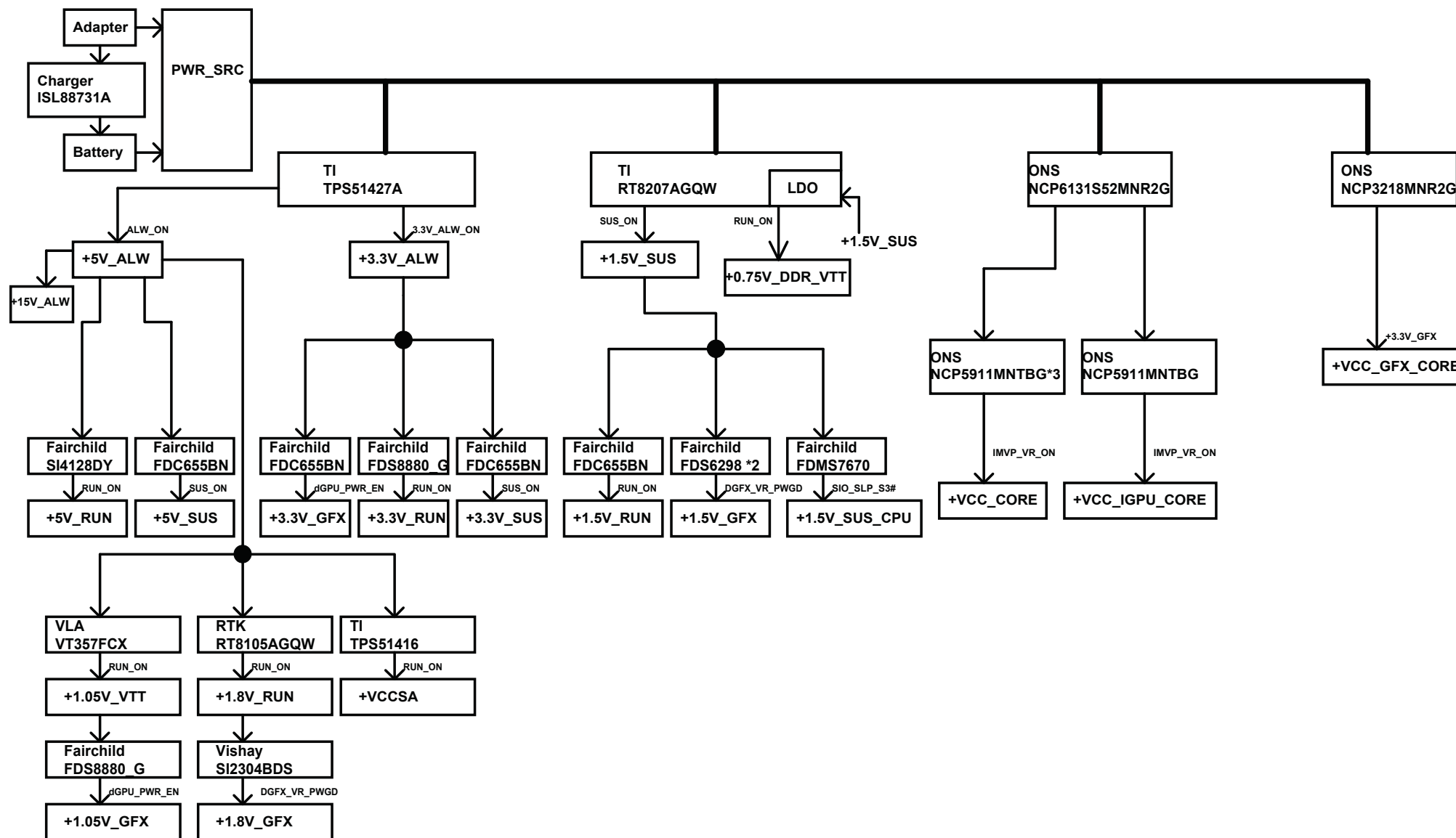




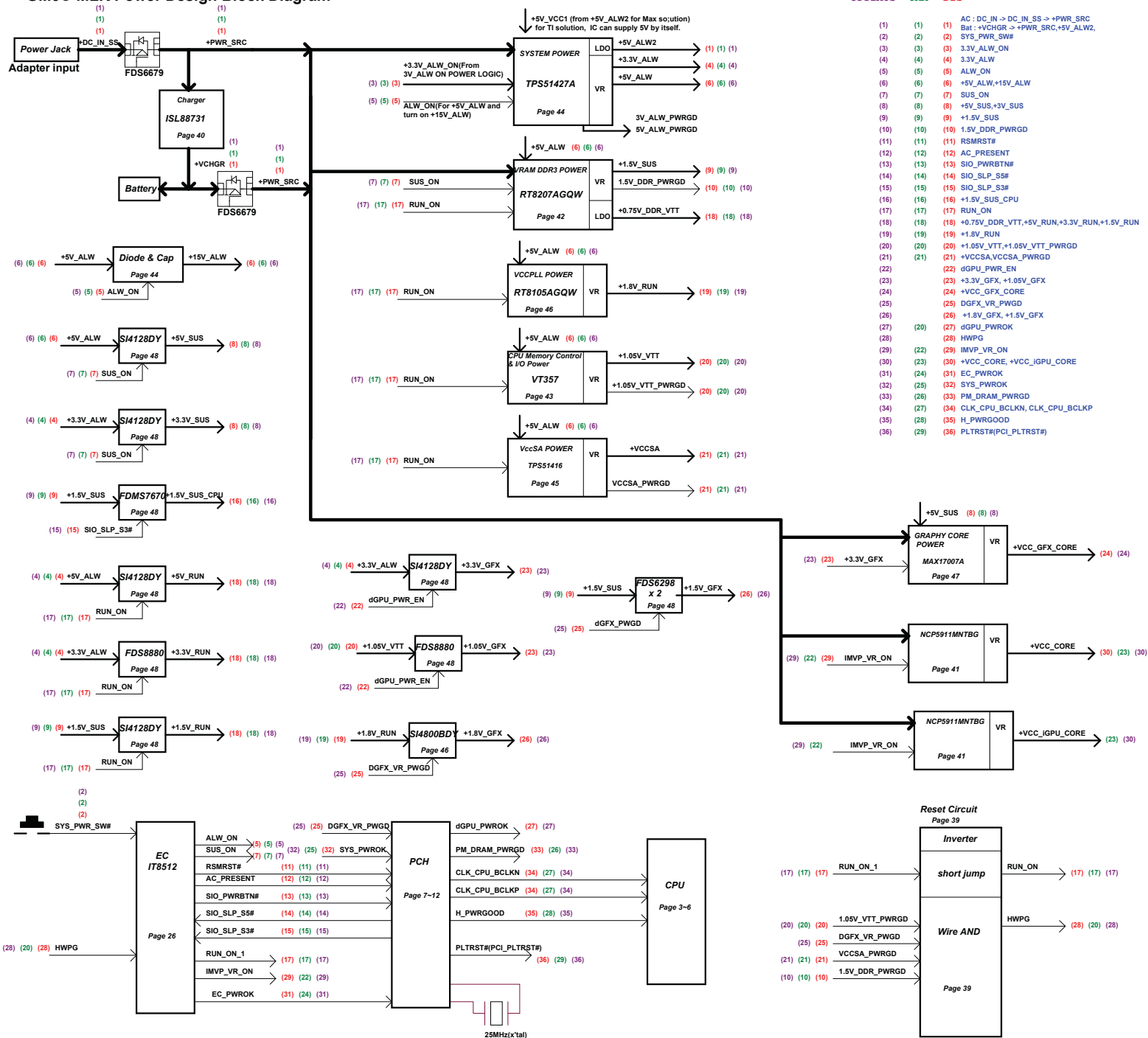


Function	IC	SMBus Address
DDR3	DIMM0	A0
	DIMM1	A4
VGA	N11P	9E
Thermal IC	EMC2112	0011100xb
Charge IC	BQ24765RUVR	0x12
Battery	Battery	0x37
Fall Sensor	DE351DLTR	0101110xb
WLAN	WLAN Module	X
WWAN	WWAN Module	X

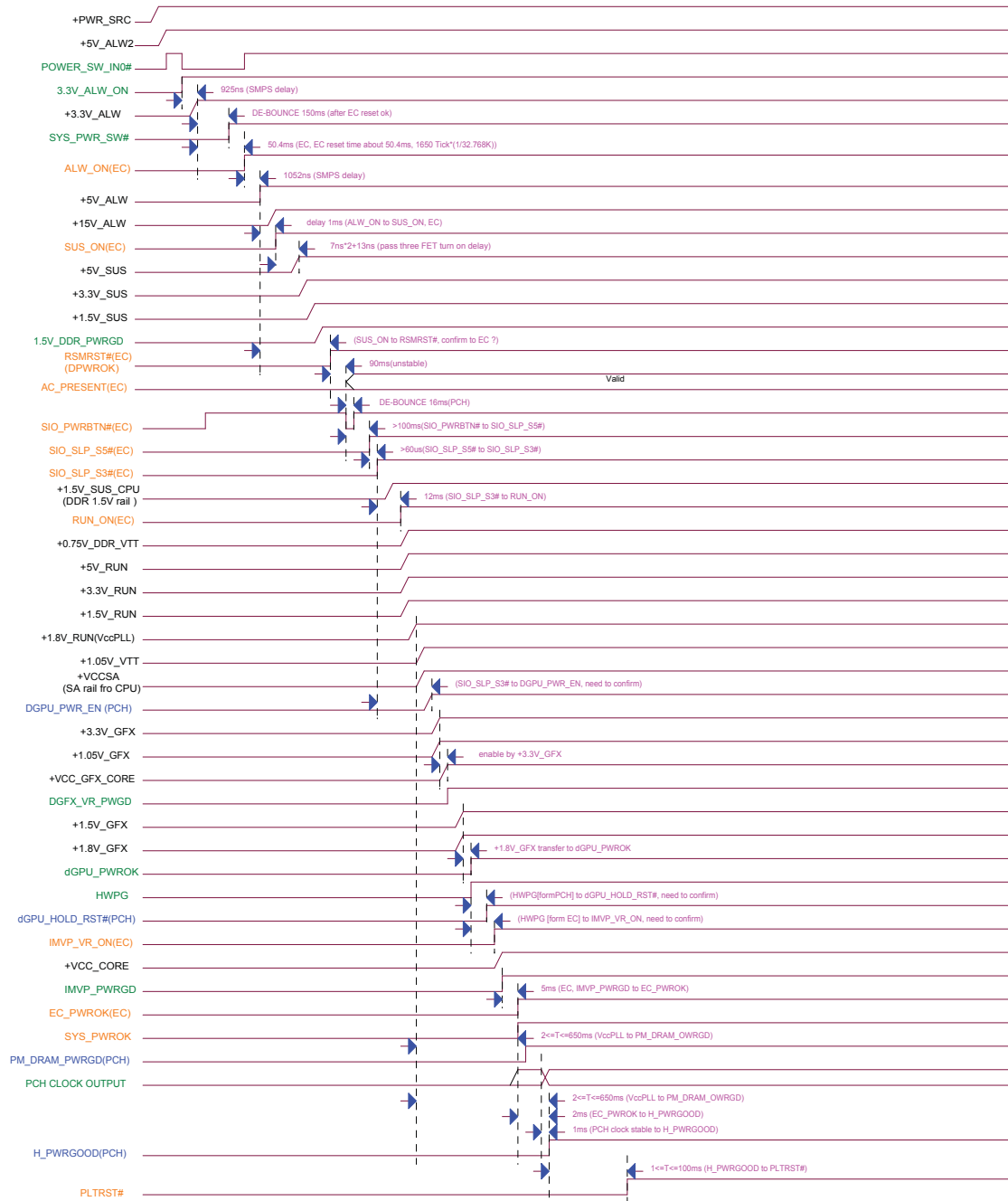




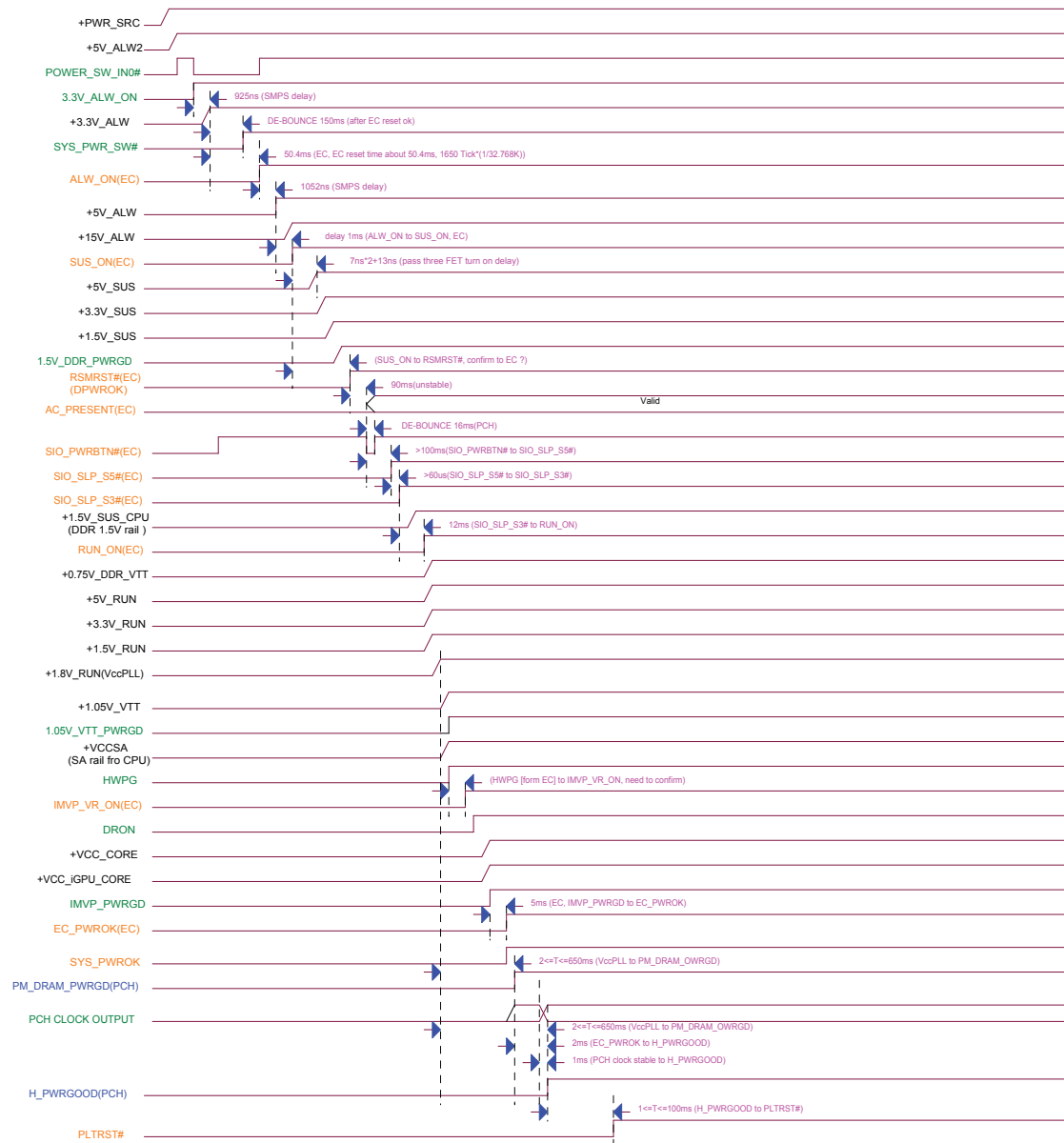
GM6C-MLK Power Design Block Diagram



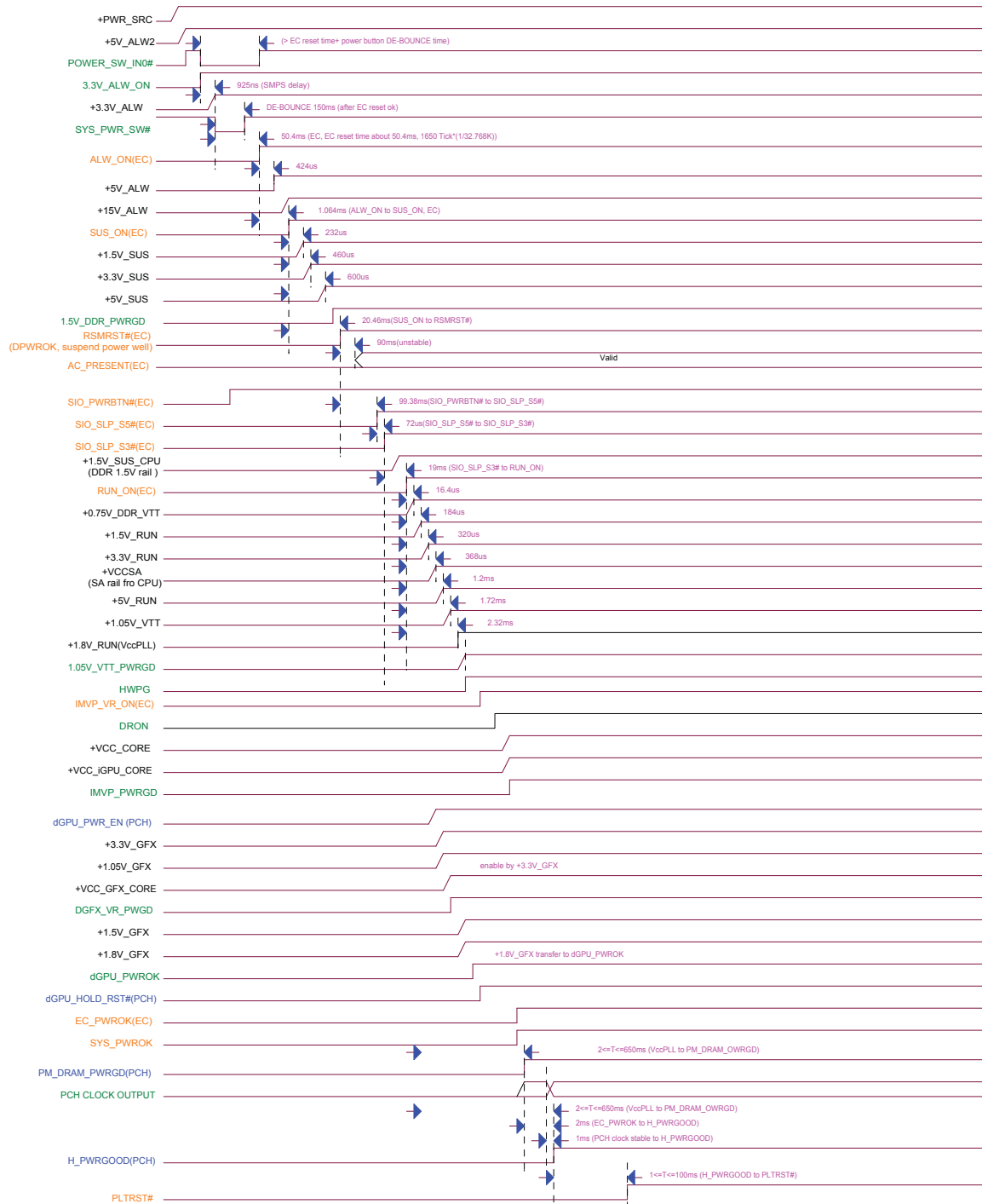
GM6C_MLK_DIS Power on Timing(BATTERY MODE)



GM6C_MLK_UMA Power on Timing(BATTERY MODE)



GM6C_MLK_OPTIMUS Power on Timing(BATTERY MODE)



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